Fig.1

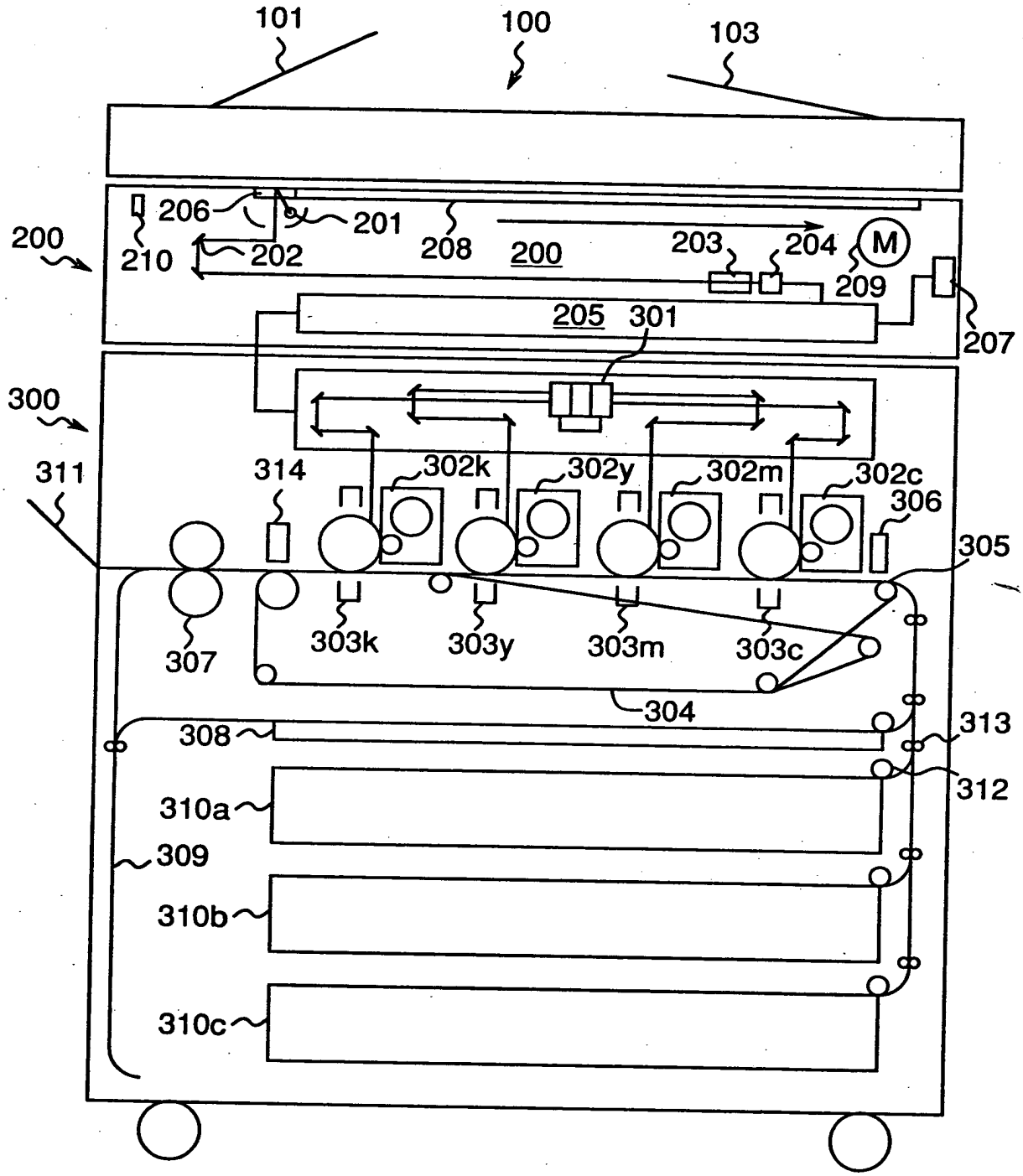

101
100
103
206
201
208
200
203
204
M
209
210
202
200
205
301
207
300
311
314
302k
302y
302m
302c
306
305
307
303k
303y
303m
303c
304
308
313
312
310a
309
310b
310c

Fig.2

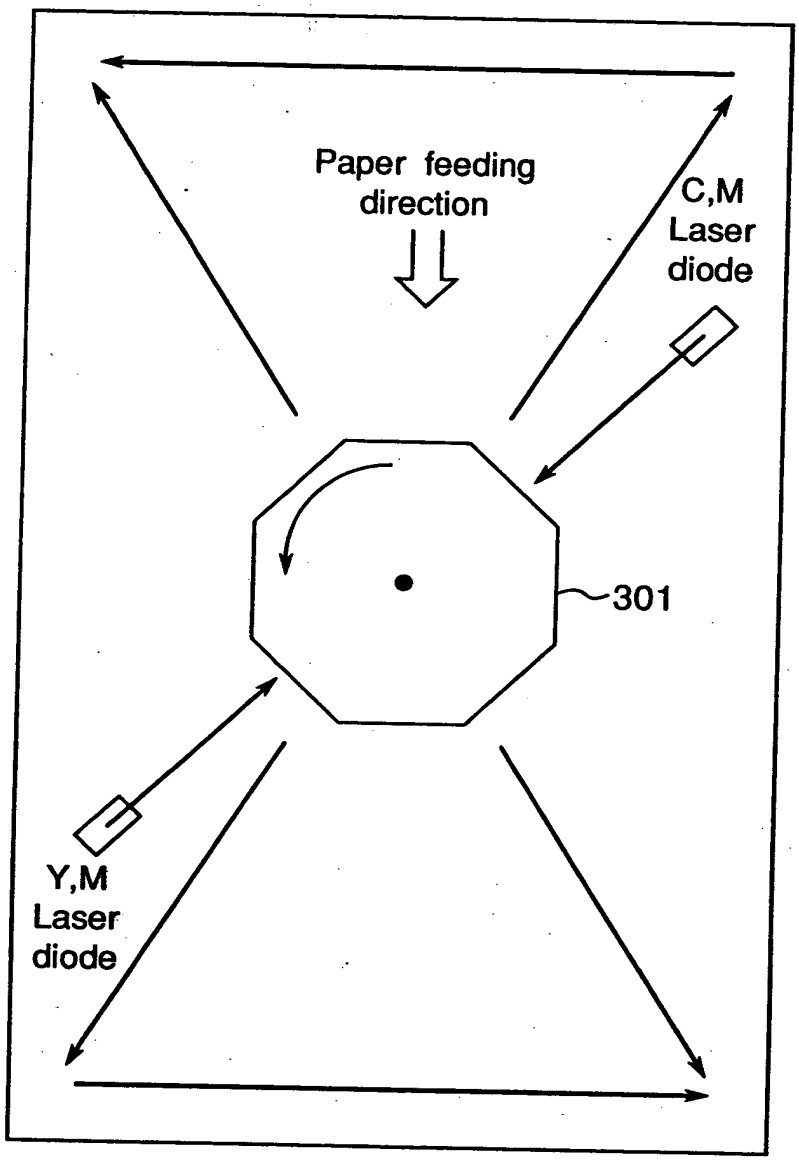
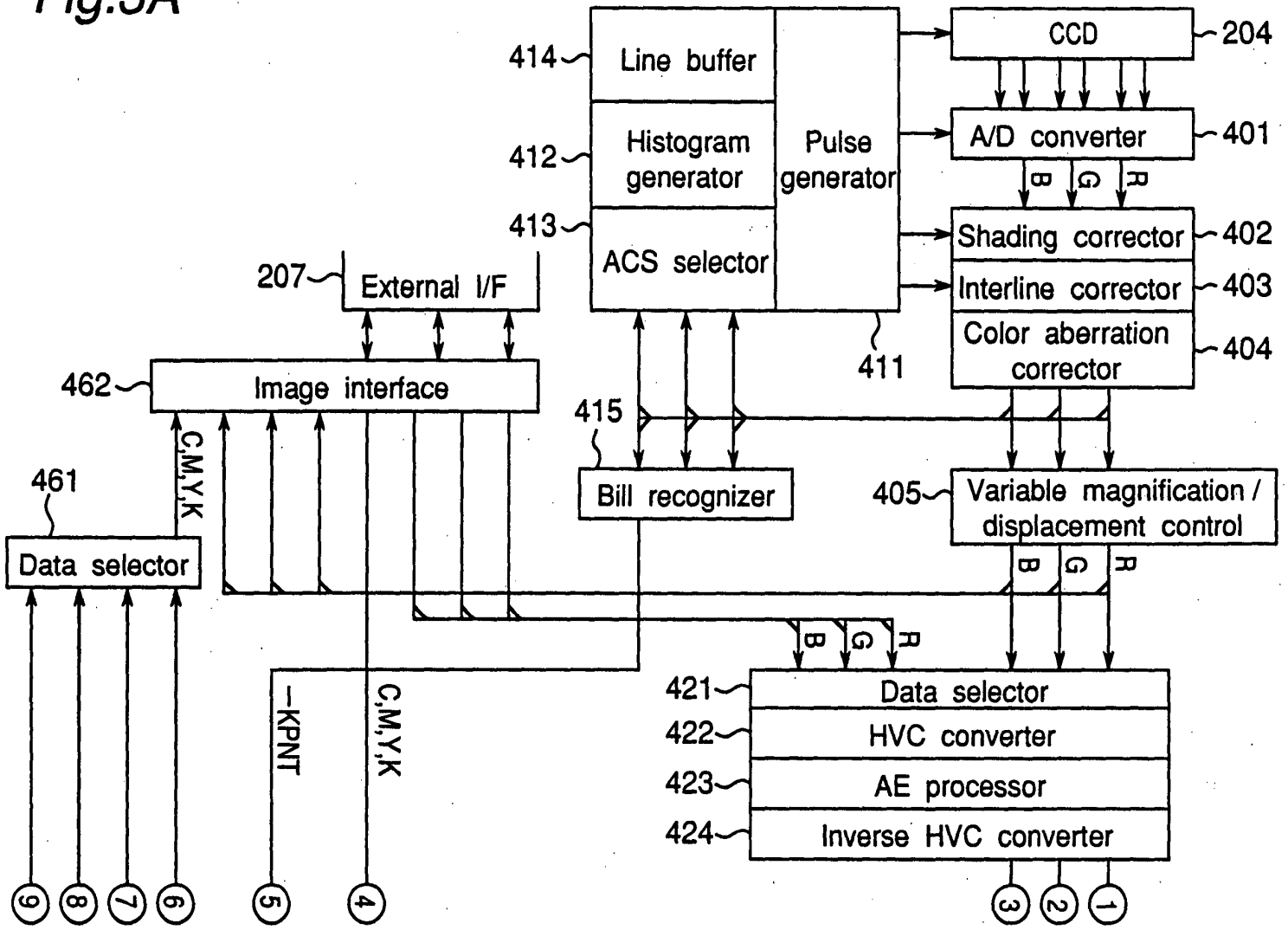


Fig.3A


414
Line buffer
412
Histogram generator
413
ACS selector
Pulse generator
411
CCD
204
A/D converter
401
B
G
R
Shading corrector
402
Interline corrector
403
Color aberration corrector
404
207
External I/F
462
Image interface
415
Bill recognizer
405
Variable magnification / displacement control
461
C,M,Y,K
Data selector
421
Data selector
422
HVC converter
423
AE processor
424
Inverse HVC converter
-KPNT
C,M,Y,K
9
8
7
6
5
4
3
2
1

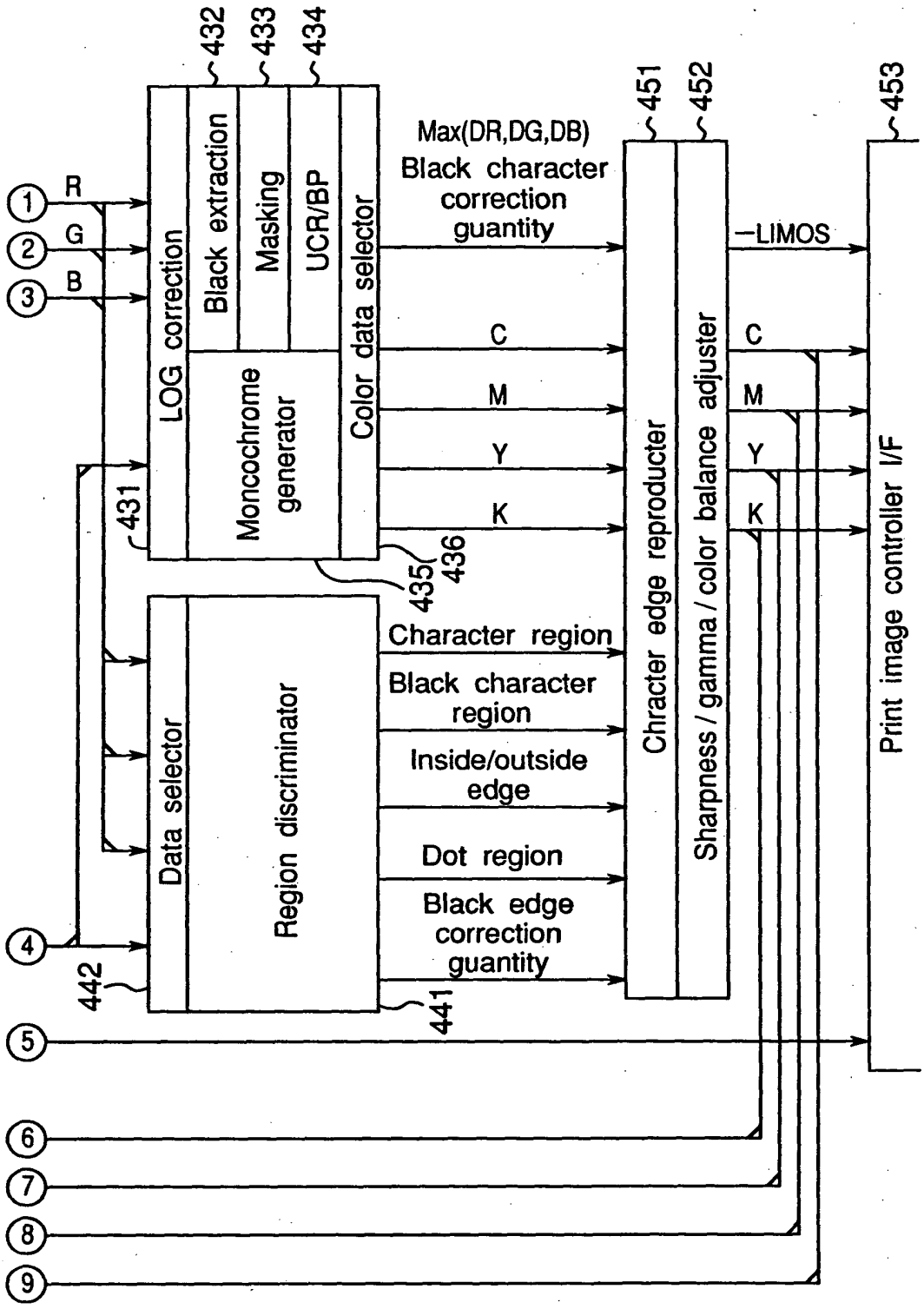

R
G
B
LOG correction
Black extraction
Masking
UCR/BP
Color data selector
Moncochrome generator
Data selector
Region discriminator
Max(DR,DG,DB)
Black character correction guantity
C
M
Y
K
Character region
Black character region
Inside/outside edge
Dot region
Black edge correction guantity
Chracter edge reproducter
Sharpness / gamma / color balance adjuster
LIMOS
C
M
Y
K
Print image controller I/F
431
432
433
434
435
436
441
442
451
452
453
1
2
3
4
5
6
7
8
9

Fig.3B

Fig.4A

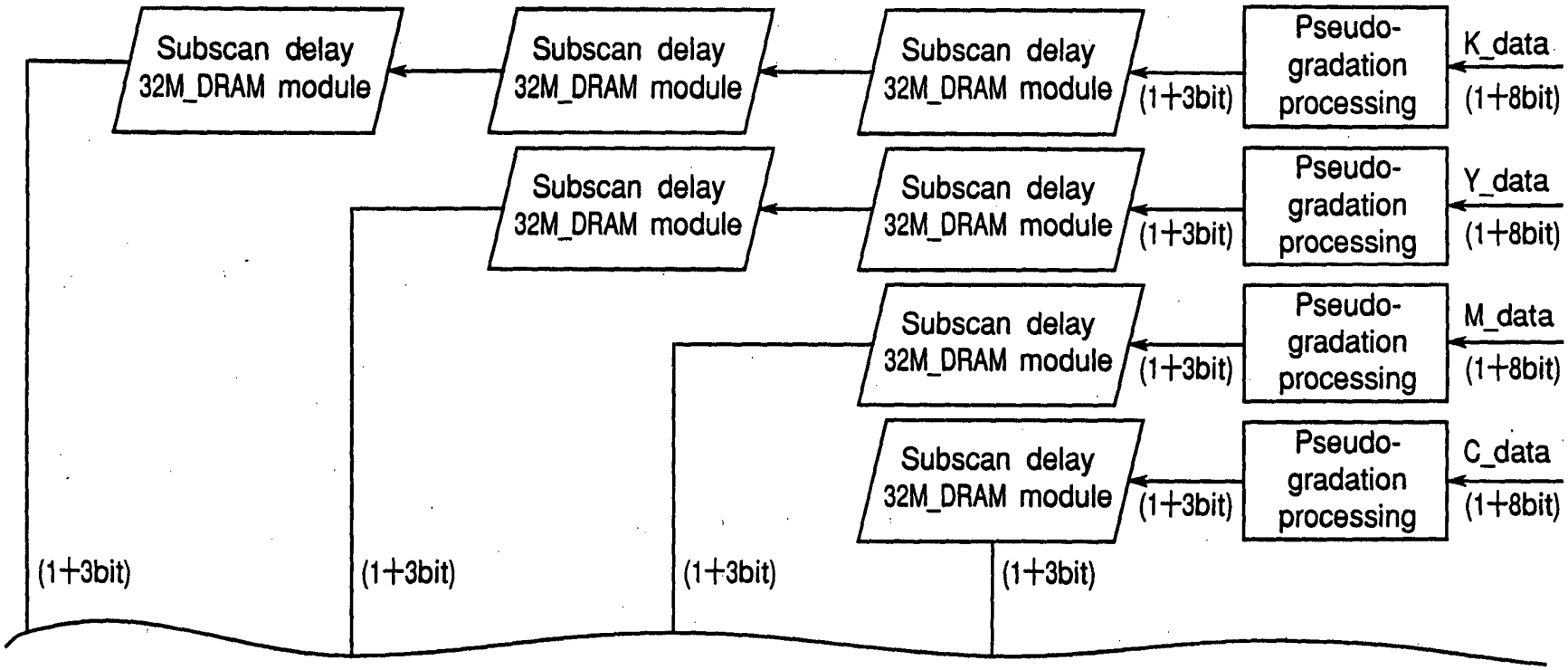

Subscan delay 32M_DRAM module
Subscan delay 32M_DRAM module
Subscan delay 32M_DRAM module
(1+3bit)
Pseudo-gradation processing
K_data
(1+8bit)
Subscan delay 32M_DRAM module
Subscan delay 32M_DRAM module
(1+3bit)
Pseudo-gradation processing
Y_data
(1+8bit)
Subscan delay 32M_DRAM module
(1+3bit)
Pseudo-gradation processing
M_data
(1+8bit)
Subscan delay 32M_DRAM module
(1+3bit)
Pseudo-gradation processing
C_data
(1+8bit)
(1+3bit)
(1+3bit)
(1+3bit)
(1+3bit)

Fig.4B

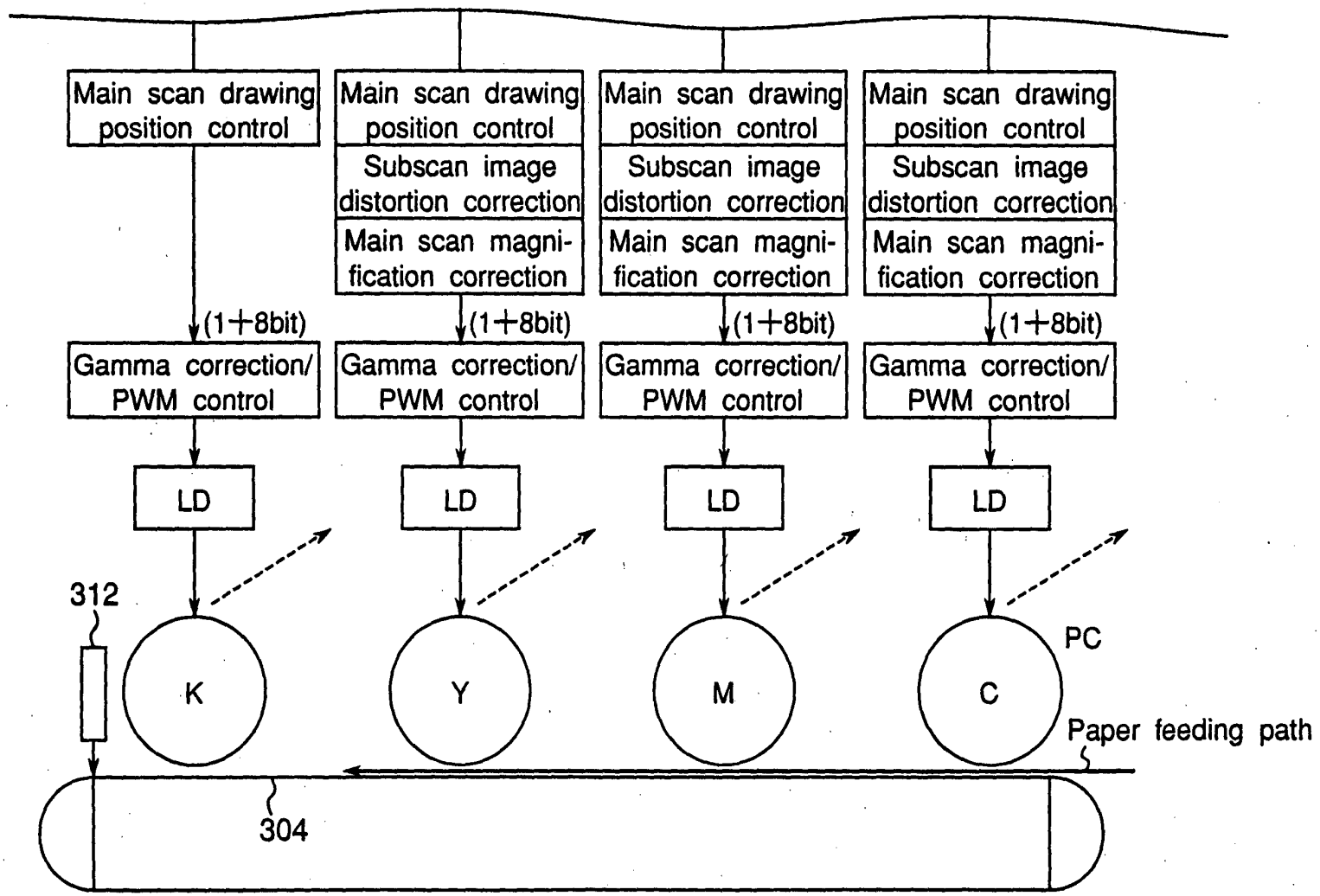
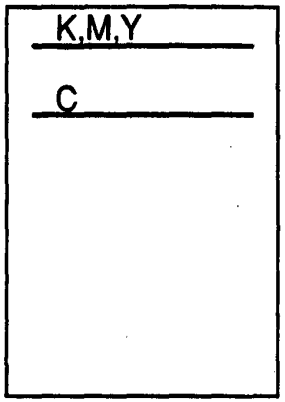
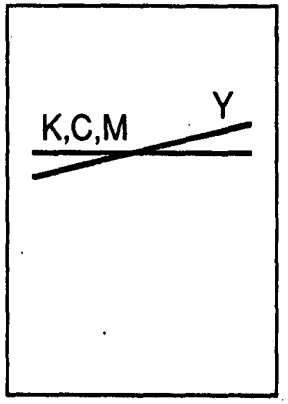

Main scan drawing position control
Subscan image distortion correction
Main scan magnification correction
(1+8bit)
Gamma correction/ PWM control
LD
312
K
Y
M
C
PC
Paper feeding path
304

Fig.5A



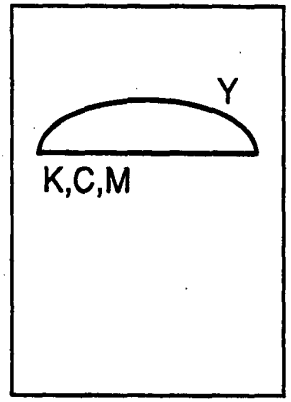
Shift of subscan drawing position

Fig.5B



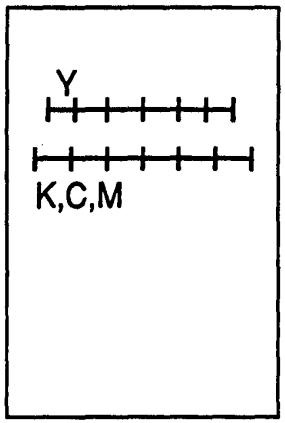
Skew

Fig.5C



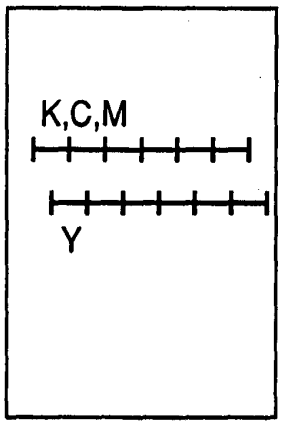
Bow distortion

Fig.5D



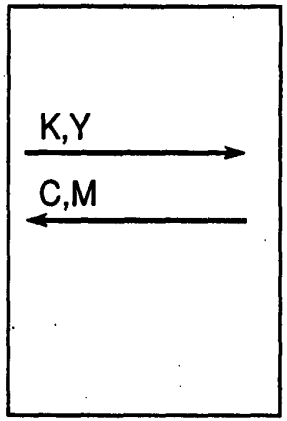
Distortion of main scan magnification

Fig.5E



Shift of main scan drawing position

Fig.5F



C,M mirror image

Fig.6

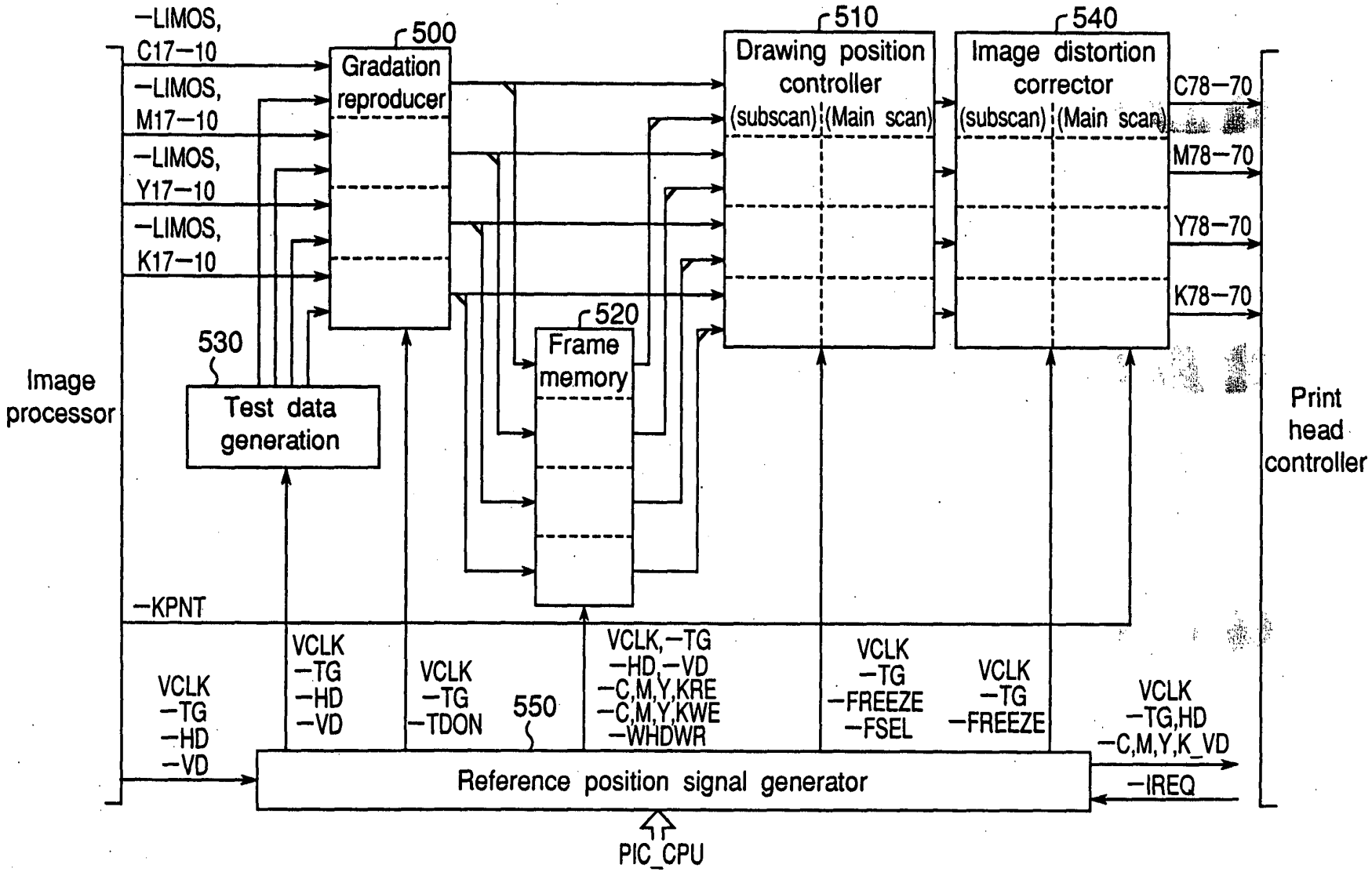

−LIMOS, C17−10
−LIMOS, M17−10
−LIMOS, Y17−10
−LIMOS, K17−10
500
Gradation reproducer
510
Drawing position controller
(subscan) (Main scan)
540
Image distortion corrector
(subscan) (Main scan)
C78−70
M78−70
Y78−70
K78−70
520
Frame memory
530
Test data generation
Image processor
Print head controller
−KPNT
VCLK −TG −HD −VD
VCLK −TG −HD −VD
VCLK −TG −TDON
550
VCLK,−TG −HD,−VD −C,M,Y,KRE −C,M,Y,KWE −WHDWR
VCLK −TG −FREEZE −FSEL
VCLK −TG −FREEZE
VCLK −TG,HD −C,M,Y,K_VD
−IREQ
Reference position signal generator
PIC_CPU

Fig.7

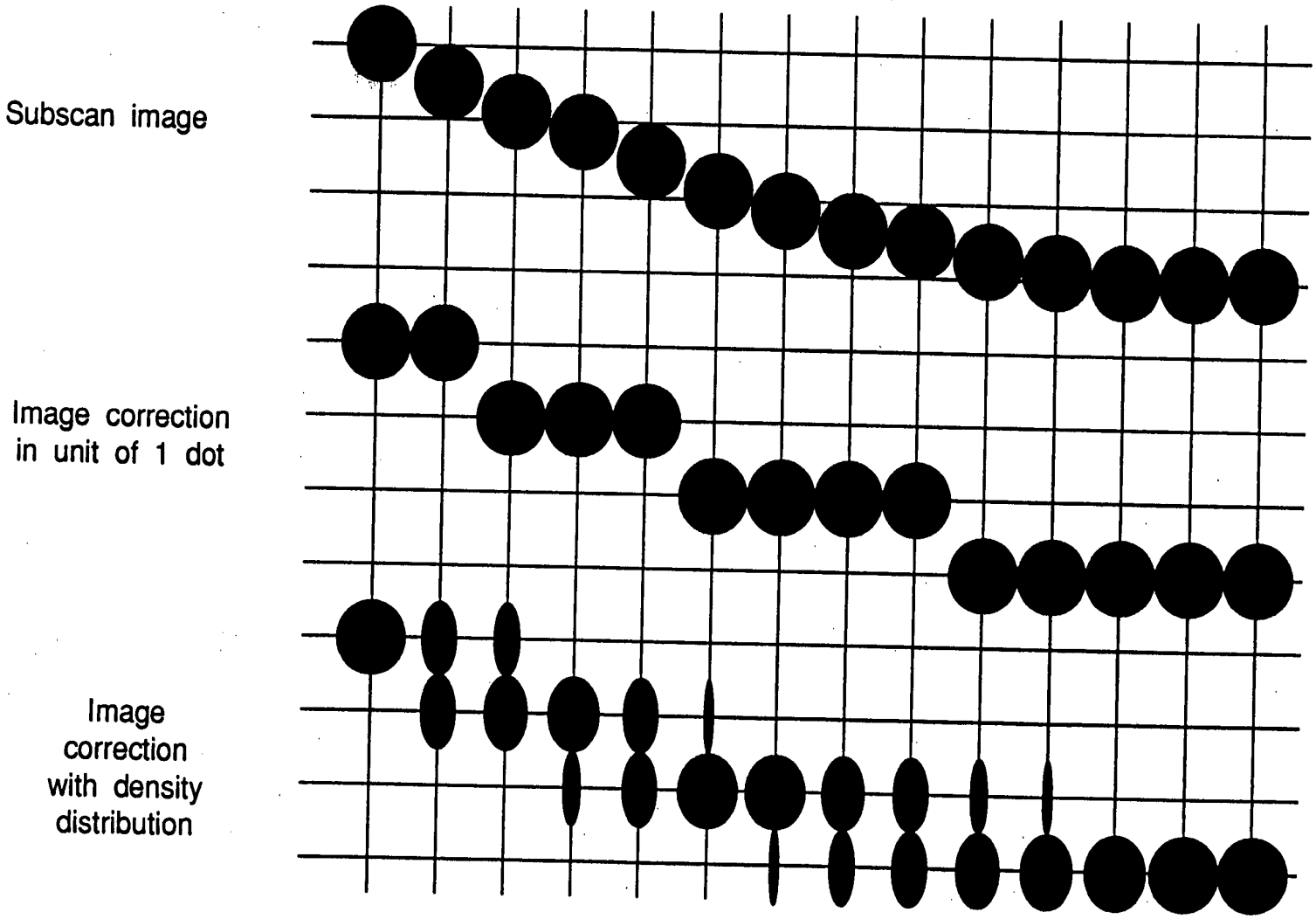

Subscan image
Image correction in unit of 1 dot
Image correction with density distribution

Fig.8

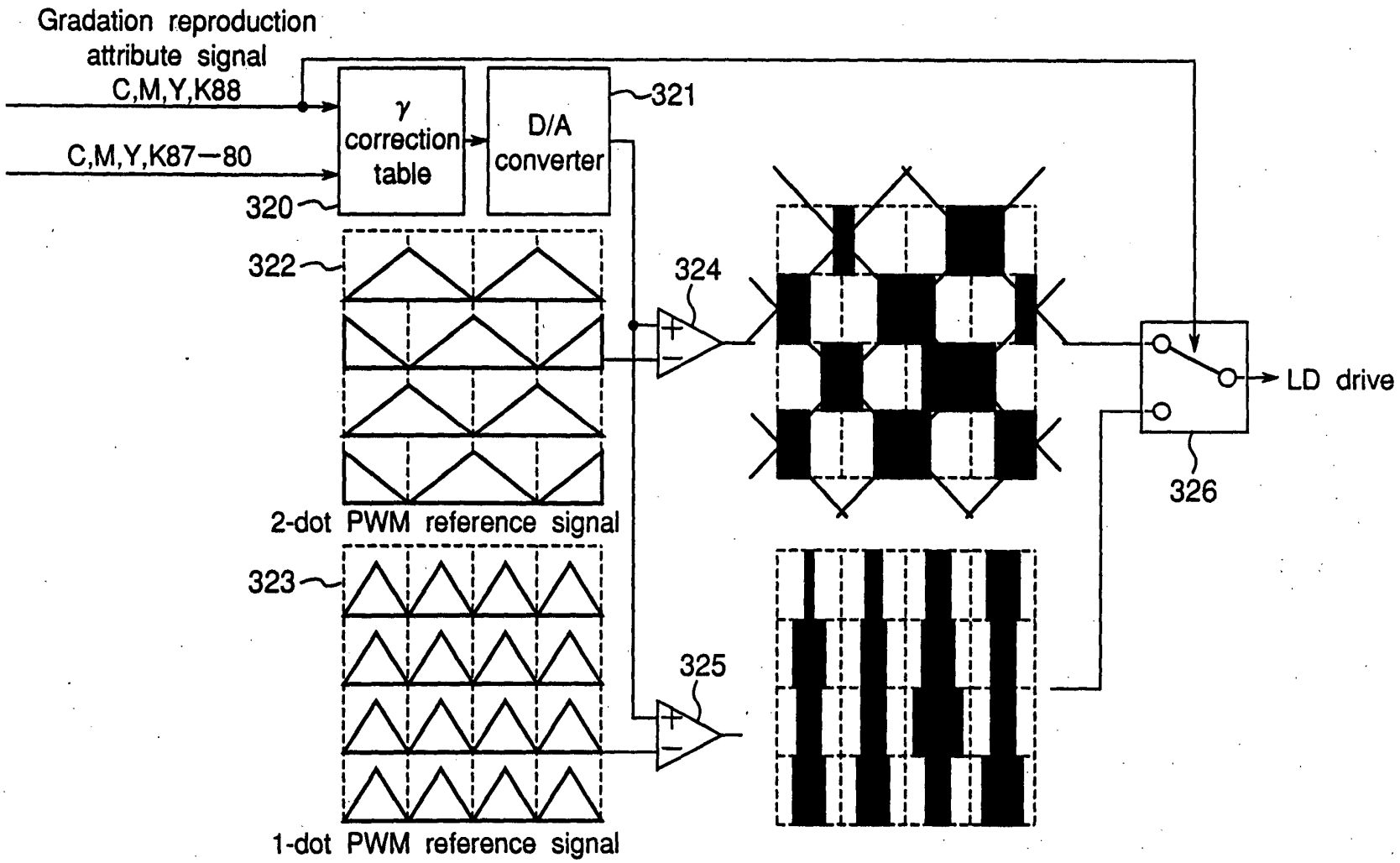

Gradation reproduction attribute signal C,M,Y,K88
C,M,Y,K87—80
γ correction table
D/A converter
321
320
322
324
2-dot PWM reference signal
323
325
1-dot PWM reference signal
326
LD drive

Fig.9

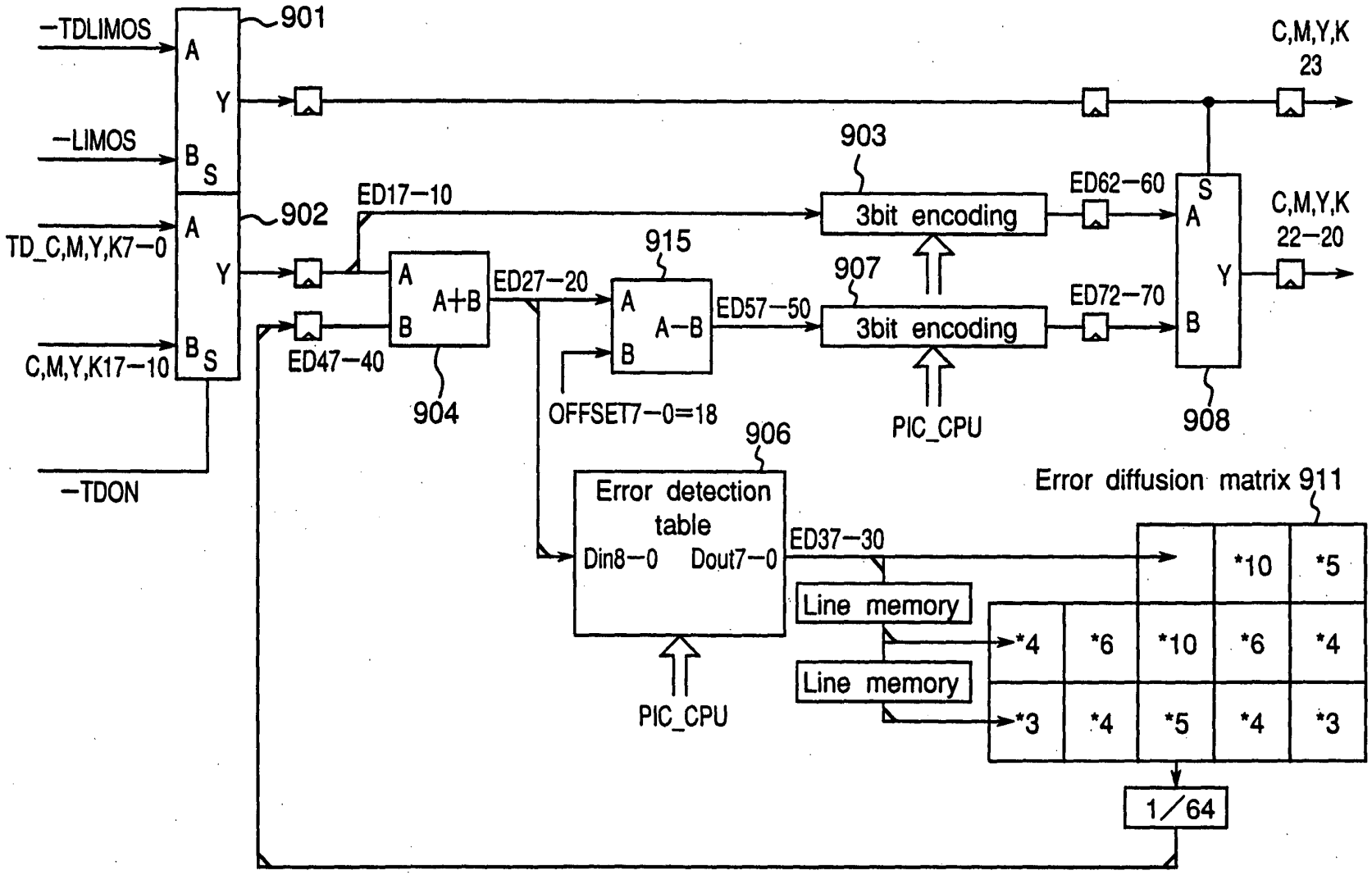

-TDLIMOS
-LIMOS
TD_C,M,Y,K7-0
C,M,Y,K17-10
-TDON
A
Y
B
S
901
902
ED17-10
ED47-40
A
A+B
B
904
ED27-20
915
A
A-B
B
OFFSET7-0=18
903
3bit encoding
907
3bit encoding
PIC_CPU
ED62-60
ED72-70
S
A
Y
B
908
C,M,Y,K
23
C,M,Y,K
22-20
906
Error detection
table
Din8-0
Dout7-0
PIC_CPU
ED37-30
Line memory
Line memory
Error diffusion matrix 911
*10
*5
*4
*6
*10
*6
*4
*3
*4
*5
*4
*3
1/64

Fig.10

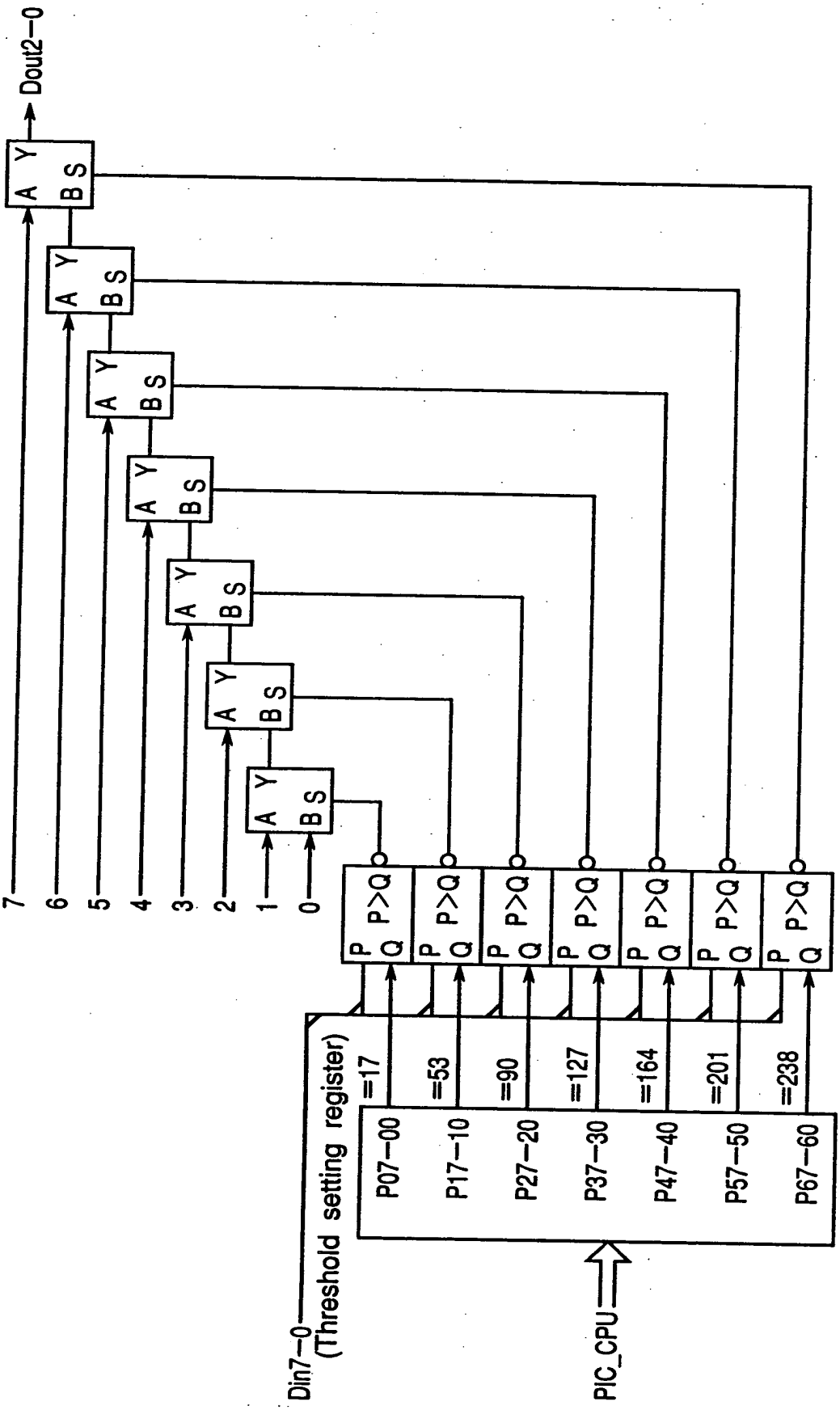

Dout2–0
A Y
B S
7
6
5
4
3
2
1
0
P P>Q
Q
Din7–0
(Threshold setting register)
P07–00
P17–10
P27–20
P37–30
P47–40
P57–50
P67–60
=17
=53
=90
=127
=164
=201
=238
PIC_CPU

Fig.11A

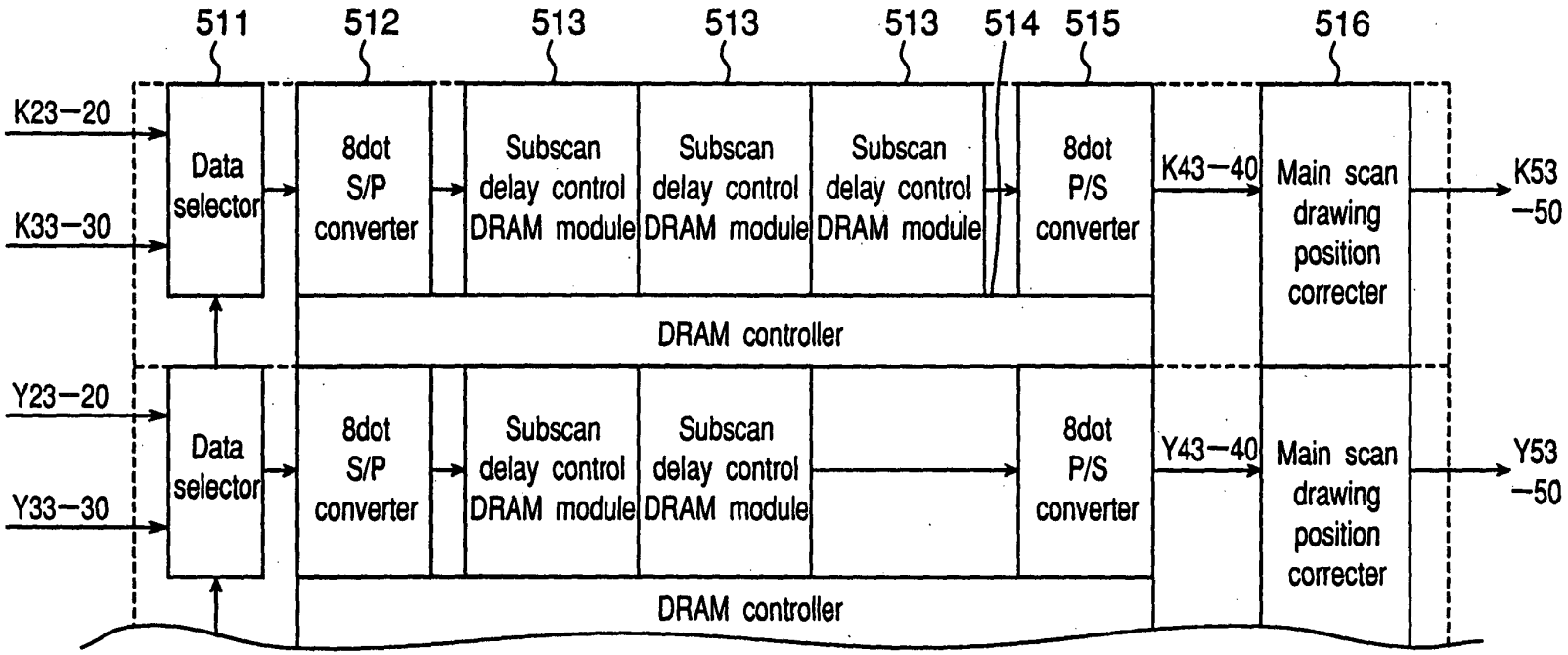

511
512
513
513
513
514
515
516
K23–20
K33–30
Data selector
8dot S/P converter
Subscan delay control DRAM module
Subscan delay control DRAM module
Subscan delay control DRAM module
8dot P/S converter
K43–40
Main scan drawing position correcter
K53 –50
DRAM controller
Y23–20
Y33–30
Data selector
8dot S/P converter
Subscan delay control DRAM module
Subscan delay control DRAM module
8dot P/S converter
Y43–40
Main scan drawing position correcter
Y53 –50
DRAM controller

Fig.11B

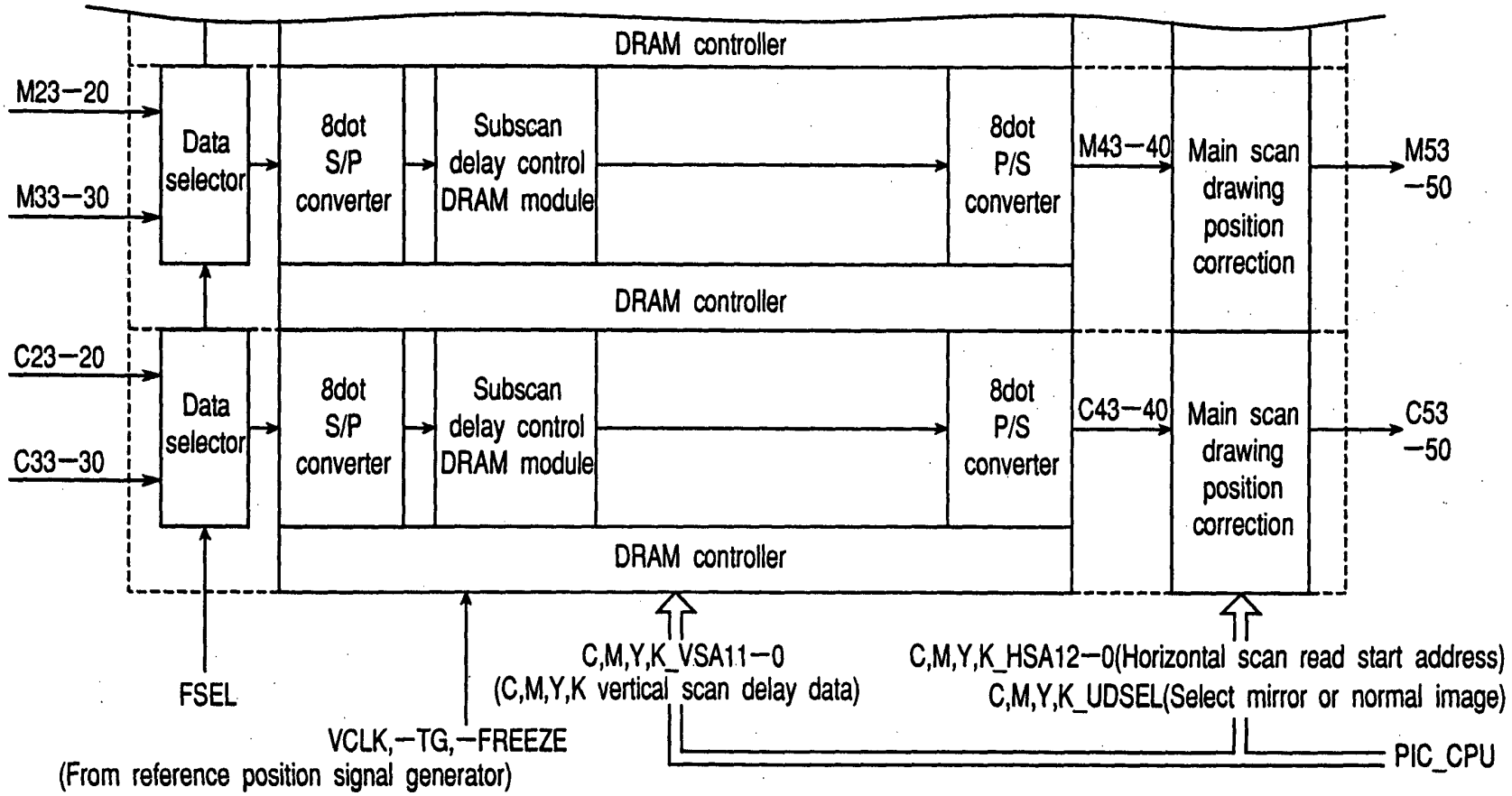

DRAM controller
M23−20
M33−30
Data selector
8dot S/P converter
Subscan delay control DRAM module
8dot P/S converter
M43−40
Main scan drawing position correction
M53 −50
DRAM controller
C23−20
C33−30
Data selector
8dot S/P converter
Subscan delay control DRAM module
8dot P/S converter
C43−40
Main scan drawing position correction
C53 −50
DRAM controller
FSEL
VCLK,−TG,−FREEZE
(From reference position signal generator)
C,M,Y,K_VSA11−0
(C,M,Y,K vertical scan delay data)
C,M,Y,K_HSA12−0(Horizontal scan read start address)
C,M,Y,K_UDSEL(Select mirror or normal image)
PIC_CPU

Fig.11C

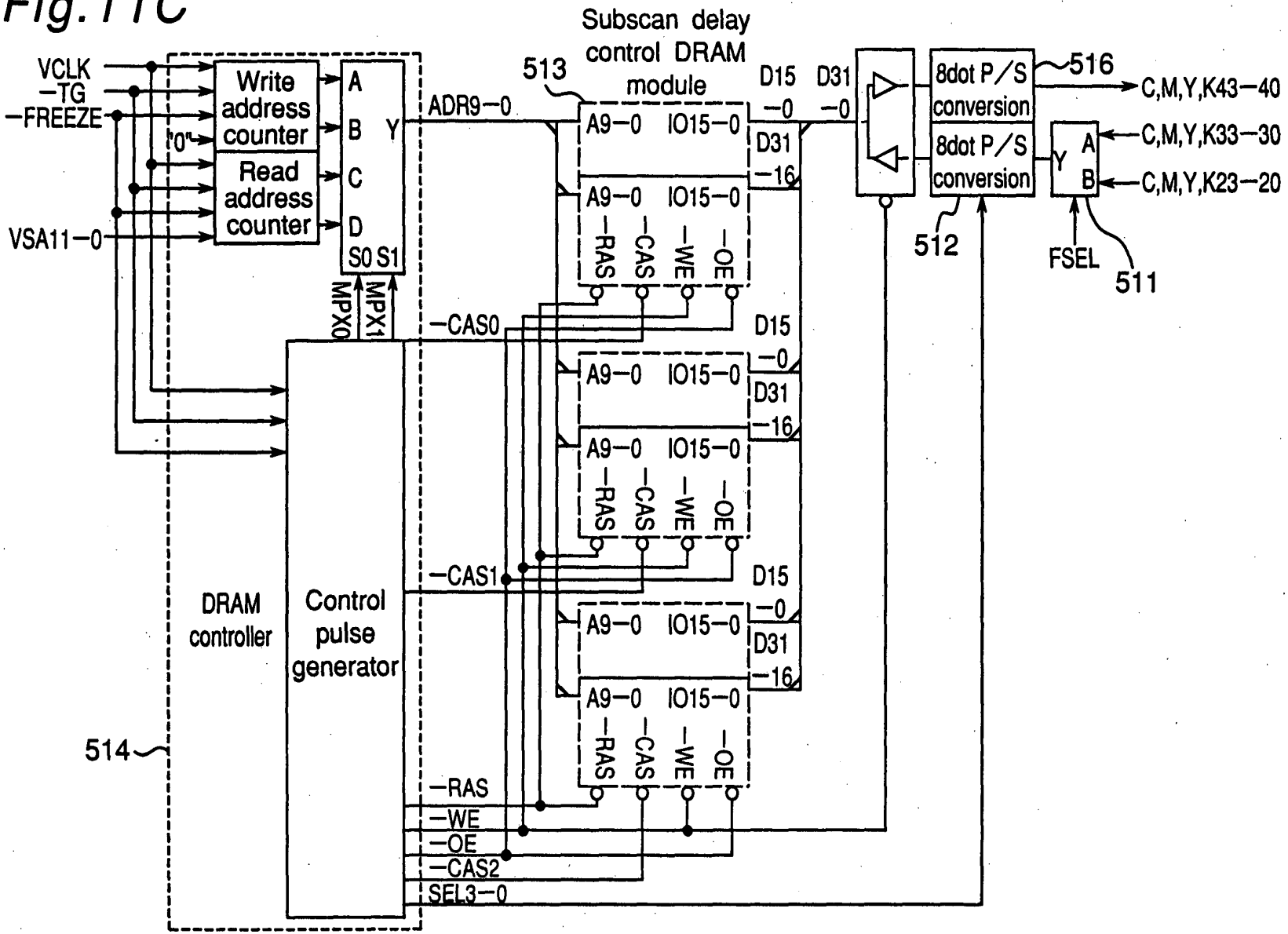

VCLK
−TG
−FREEZE
VSA11−0
Write address counter
Read address counter
"0"
A
B
C
D
Y
S0 S1
MPX0
MPX1
ADR9−0
513
Subscan delay control DRAM module
A9−0
IO15−0
−RAS
−CAS
−WE
−OE
D15
−0
D31
−16
−CAS0
−CAS1
−RAS
−WE
−OE
−CAS2
SEL3−0
DRAM controller
Control pulse generator
514
8dot P/S conversion
8dot P/S conversion
516
512
FSEL
511
C,M,Y,K43−40
C,M,Y,K33−30
C,M,Y,K23−20

Fig. 12

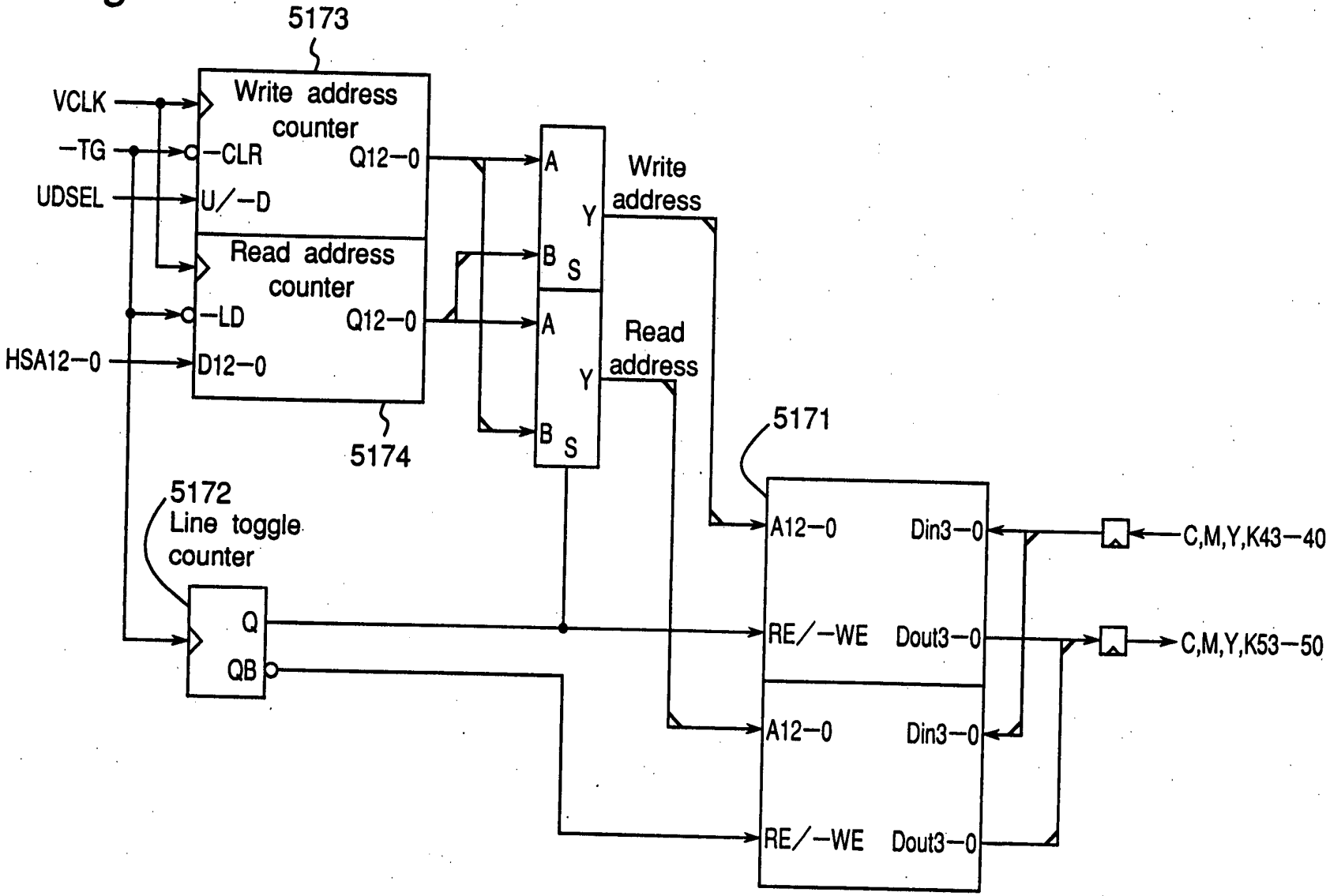

5173
Write address counter
VCLK
−TG
−CLR
Q12−0
UDSEL
U/−D
Read address counter
−LD
Q12−0
HSA12−0
D12−0
5174
A
Y
B
S
Write address
Read address
5171
5172
Line toggle counter
Q
QB
A12−0
Din3−0
RE/−WE
Dout3−0
C,M,Y,K43−40
C,M,Y,K53−50

Fig.13A

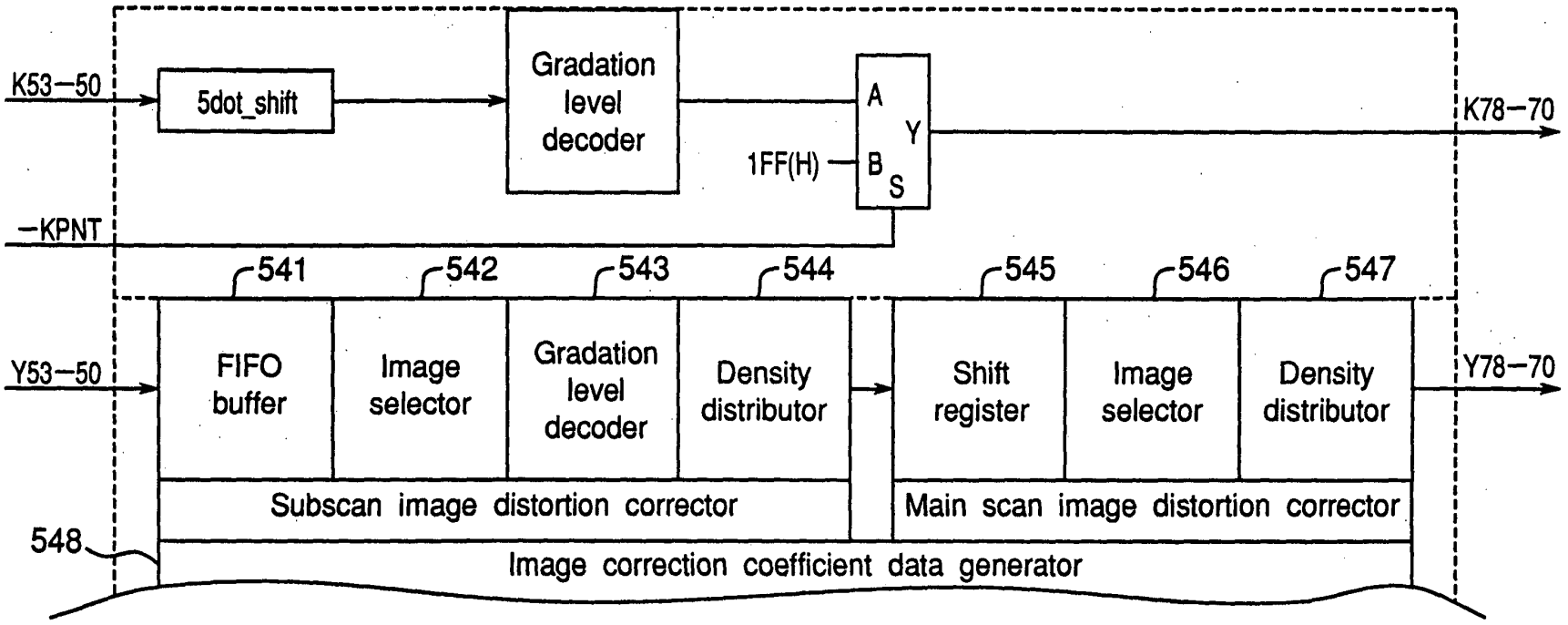

K53–50
5dot_shift
Gradation level decoder
A
Y
B
S
1FF(H)
K78–70
–KPNT
541
542
543
544
545
546
547
Y53–50
FIFO buffer
Image selector
Gradation level decoder
Density distributor
Shift register
Image selector
Density distributor
Y78–70
Subscan image distortion corrector
Main scan image distortion corrector
548
Image correction coefficient data generator

Fig.13B

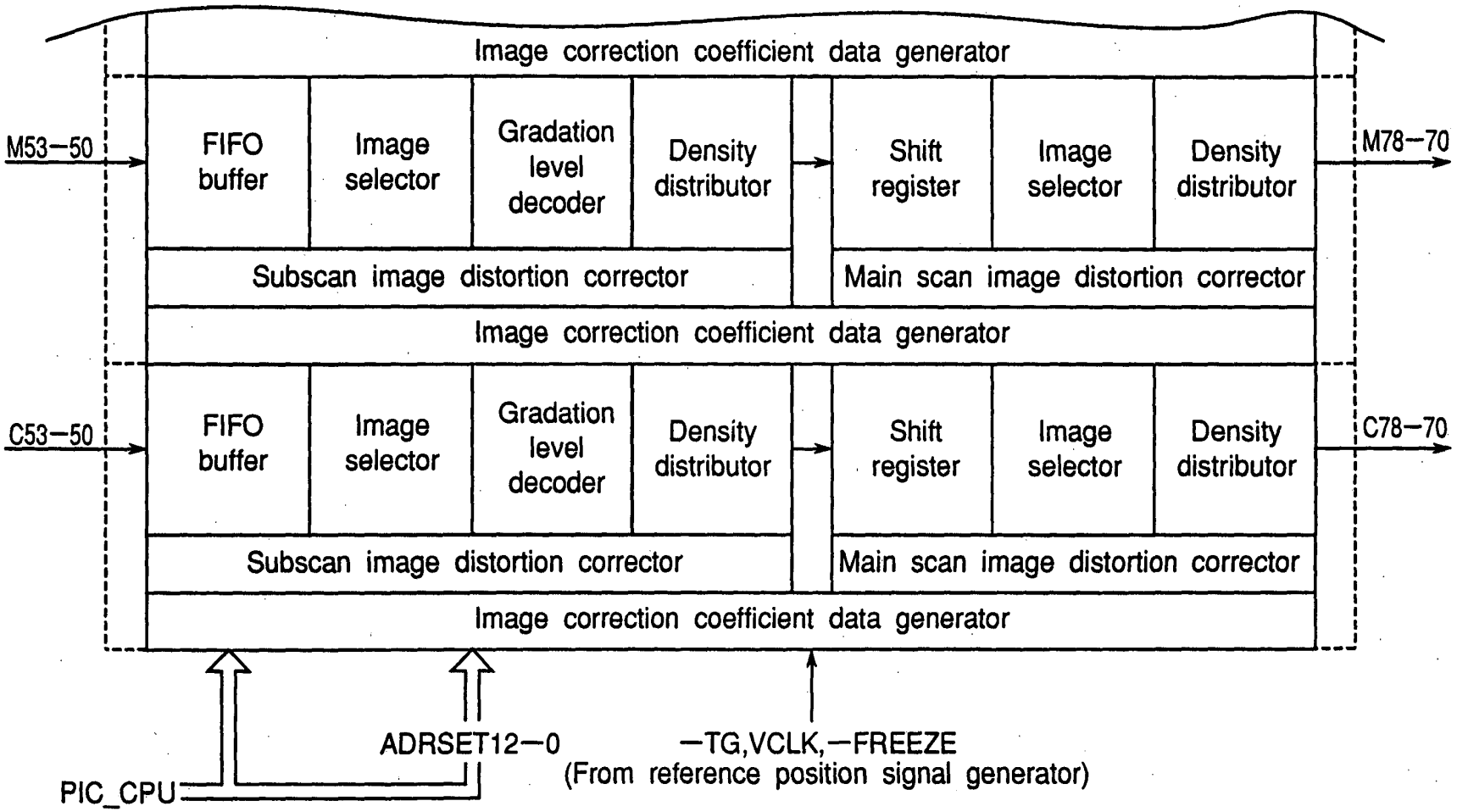


Image correction coefficient data generator
M53–50
FIFO buffer
Image selector
Gradation level decoder
Density distributor
Shift register
Image selector
Density distributor
M78–70
Subscan image distortion corrector
Main scan image distortion corrector
Image correction coefficient data generator
C53–50
FIFO buffer
Image selector
Gradation level decoder
Density distributor
Shift register
Image selector
Density distributor
C78–70
Subscan image distortion corrector
Main scan image distortion corrector
Image correction coefficient data generator
ADRSET12–0
–TG,VCLK,–FREEZE
(From reference position signal generator)
PIC_CPU

Fig.14A

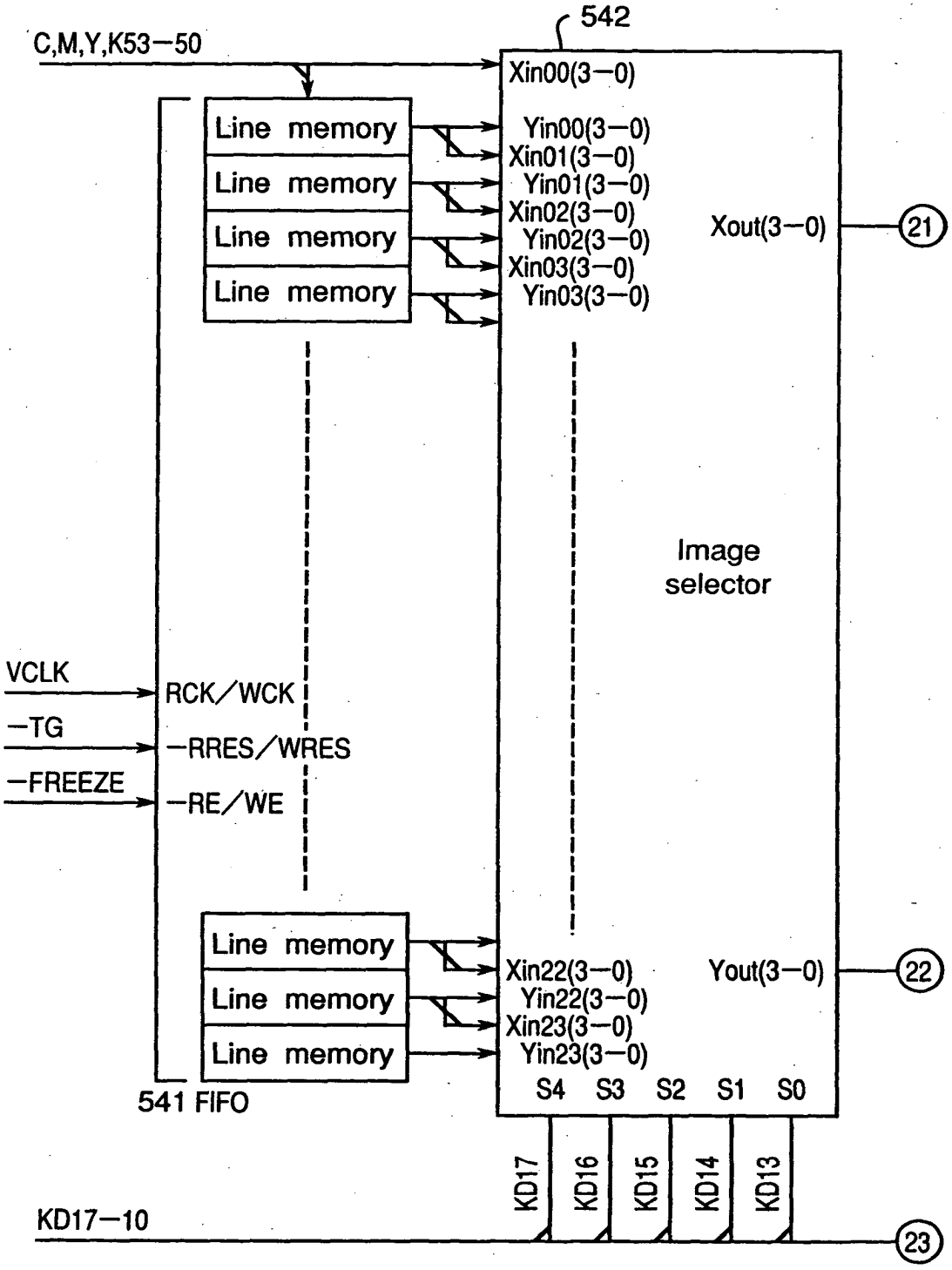

542
C,M,Y,K53−50
Xin00(3−0)
Line memory
Line memory
Line memory
Line memory
Yin00(3−0)
Xin01(3−0)
Yin01(3−0)
Xin02(3−0)
Yin02(3−0)
Xin03(3−0)
Yin03(3−0)
Xout(3−0)
21
Image selector
VCLK
RCK/WCK
−TG
−RRES/WRES
−FREEZE
−RE/WE
Line memory
Line memory
Line memory
Xin22(3−0)
Yin22(3−0)
Xin23(3−0)
Yin23(3−0)
Yout(3−0)
22
S4 S3 S2 S1 S0
541 FIFO
KD17
KD16
KD15
KD14
KD13
KD17−10
23

Fig.14B

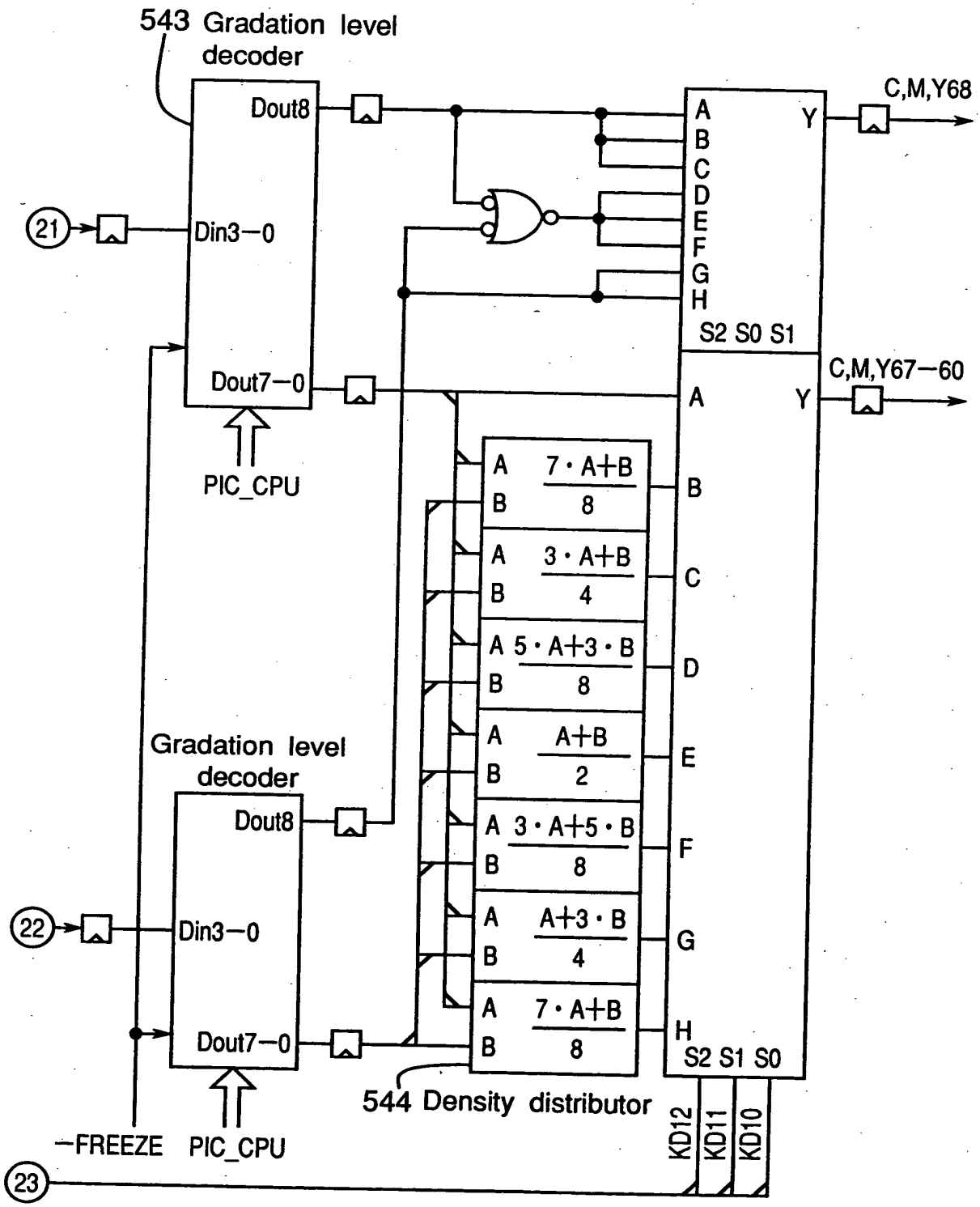

543 Gradation level decoder
Dout8
Din3–0
Dout7–0
PIC_CPU
21
22
23
Gradation level decoder
Dout8
Din3–0
Dout7–0
PIC_CPU
–FREEZE
A B C D E F G H
S2 S0 S1
Y
C,M,Y68
C,M,Y67–60
A
B
C
D
E
F
G
H
S2 S1 S0
A B 7·A+B / 8
A B 3·A+B / 4
A B 5·A+3·B / 8
A B A+B / 2
A B 3·A+5·B / 8
A B A+3·B / 4
A B 7·A+B / 8
544 Density distributor
KD12
KD11
KD10

Fig.15

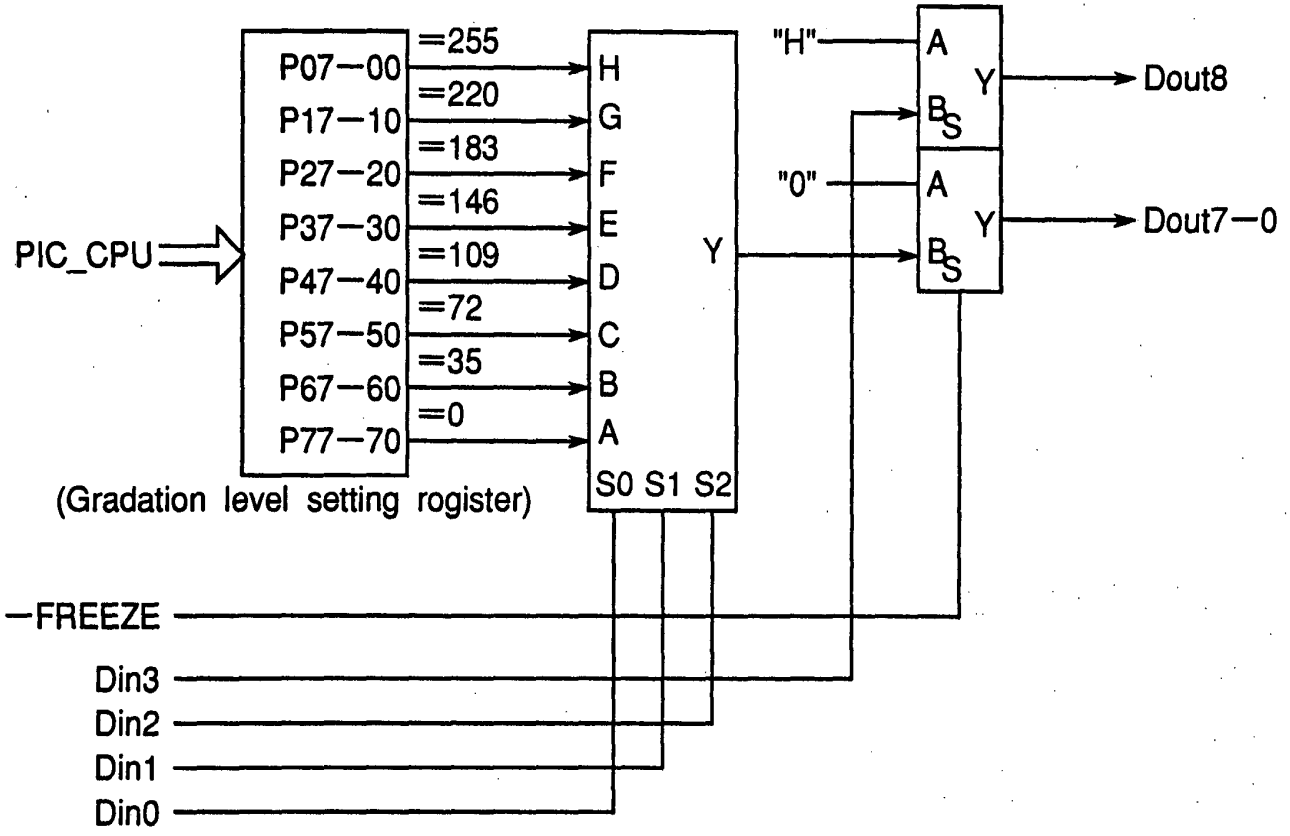

P07—00
P17—10
P27—20
P37—30
P47—40
P57—50
P67—60
P77—70
=255
=220
=183
=146
=109
=72
=35
=0
H
G
F
E
D
C
B
A
Y
S0 S1 S2
(Gradation level setting rogister)
PIC_CPU
"H"
"0"
A
B
S
Y
Dout8
Dout7—0
—FREEZE
Din3
Din2
Din1
Din0

Fig.16A

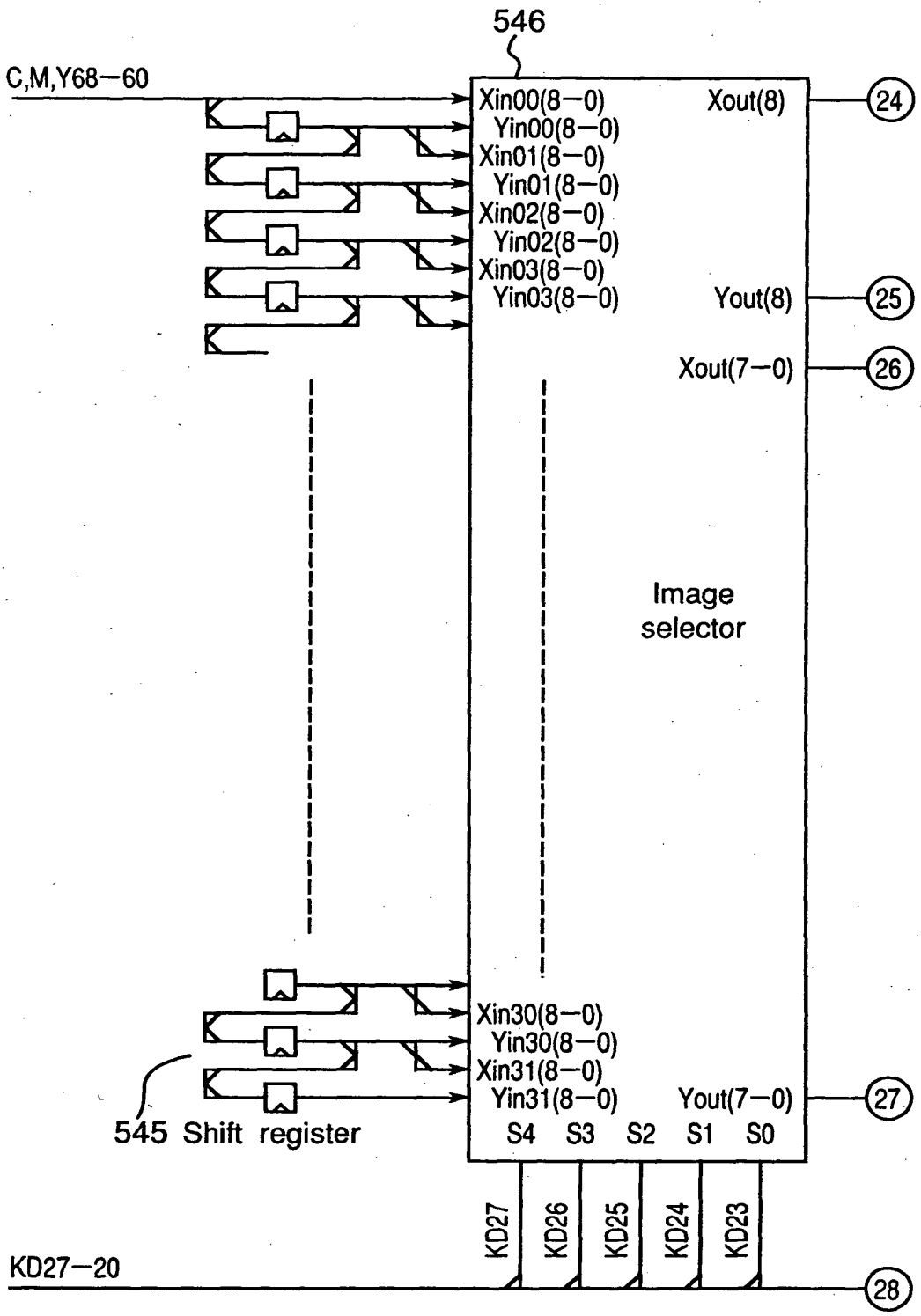

546
C,M,Y68−60
Xin00(8−0)
Yin00(8−0)
Xin01(8−0)
Yin01(8−0)
Xin02(8−0)
Yin02(8−0)
Xin03(8−0)
Yin03(8−0)
Xout(8)
24
Yout(8)
25
Xout(7−0)
26
Image selector
Xin30(8−0)
Yin30(8−0)
Xin31(8−0)
Yin31(8−0)
Yout(7−0)
27
S4 S3 S2 S1 S0
545 Shift register
KD27
KD26
KD25
KD24
KD23
KD27−20
28

Fig.16B

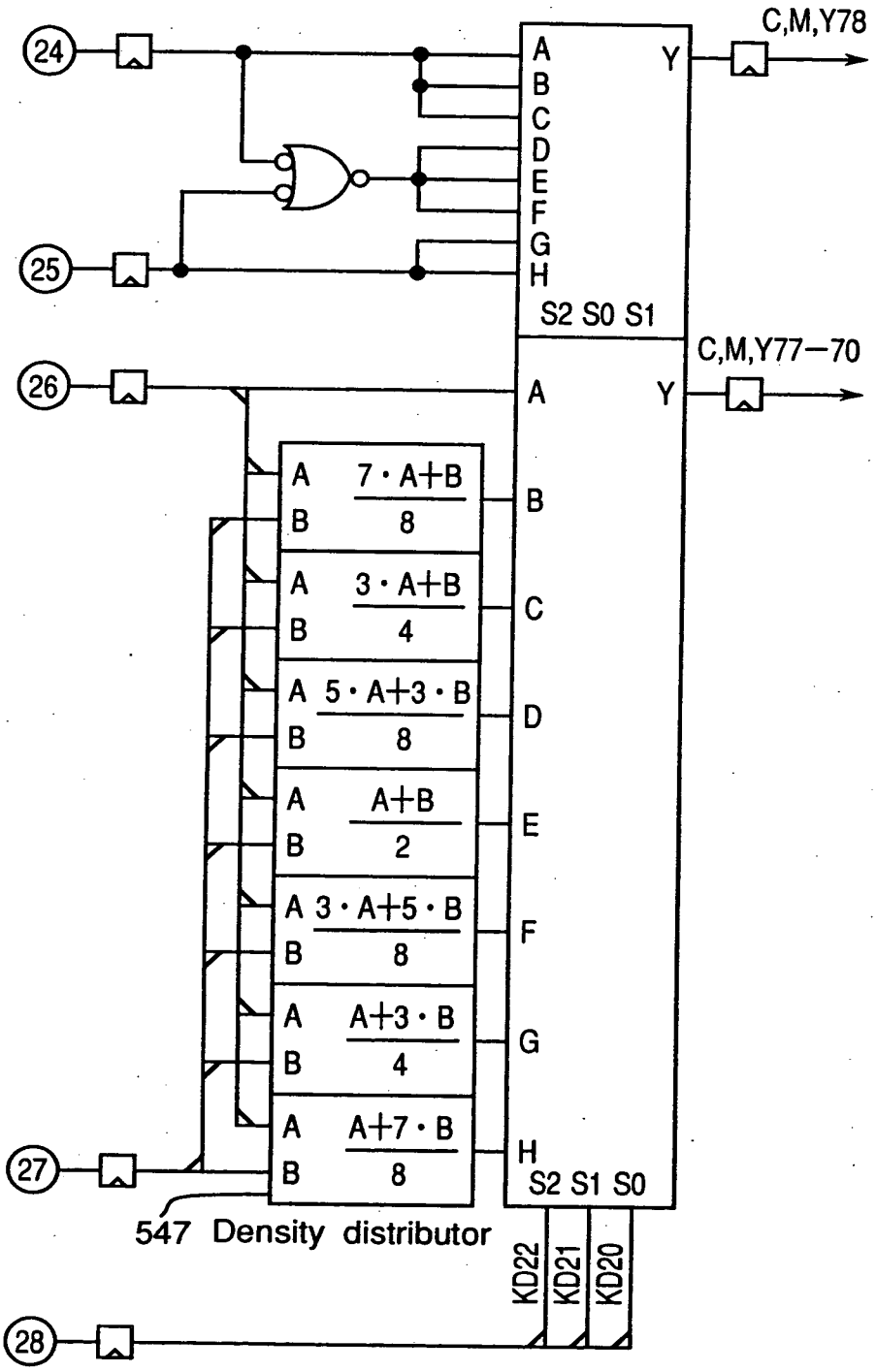

24
25
26
27
28
A
B
C
D
E
F
G
H
Y
S2 S0 S1
C,M,Y78
C,M,Y77—70
A
Y
A 7・A+B / B 8
B
A 3・A+B / B 4
C
A 5・A+3・B / B 8
D
A A+B / B 2
E
A 3・A+5・B / B 8
F
A A+3・B / B 4
G
A A+7・B / B 8
H
S2 S1 S0
547 Density distributor
KD22
KD21
KD20

Fig.17

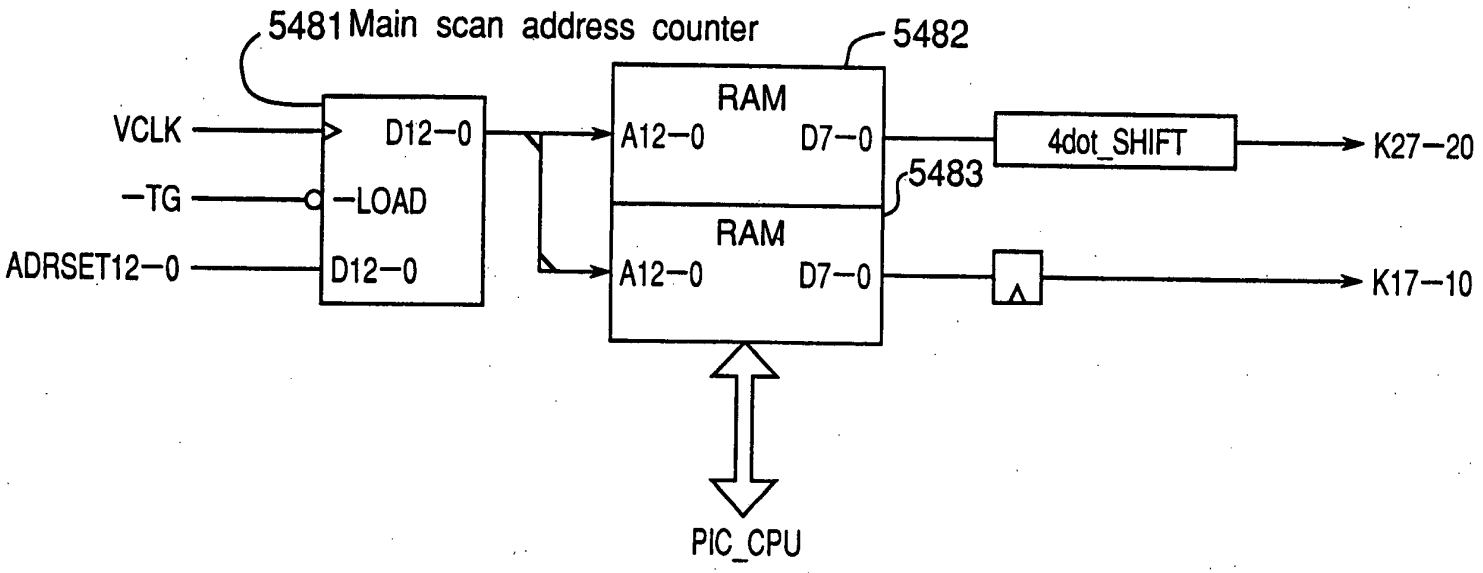
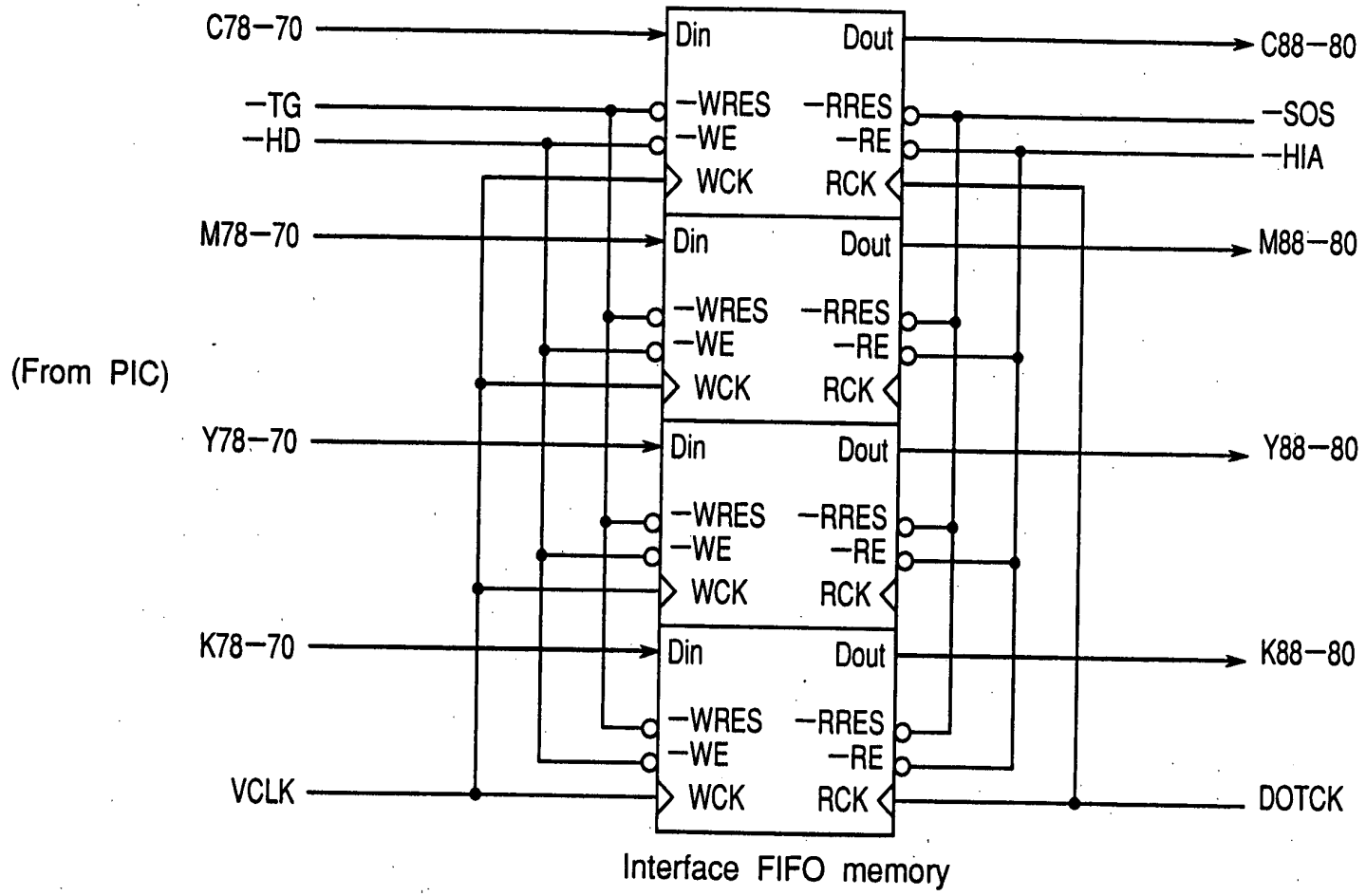

5481 Main scan address counter
5482
VCLK
D12–0
–TG
–LOAD
ADRSET12–0
D12–0
RAM
A12–0
D7–0
5483
RAM
A12–0
D7–0
4dot_SHIFT
K27–20
K17–10
PIC_CPU

Fig.18



Interface FIFO memory

Fig. 19

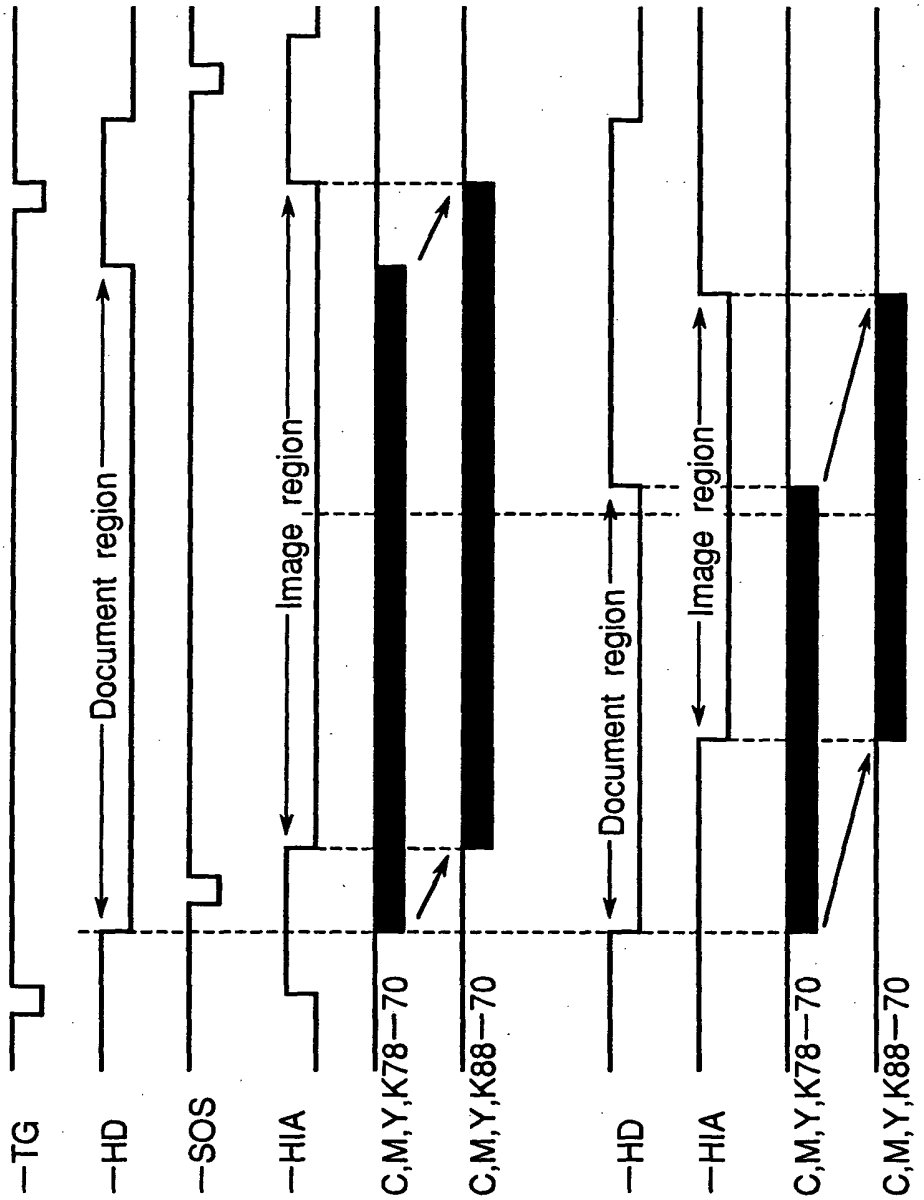

—TG
—HD
Document region
—SOS
—HIA
Image region
C,M,Y,K78—70
C,M,Y,K88—70
—HD
Document region
—HIA
Image region
C,M,Y,K78—70
C,M,Y,K88—70

Fig.20

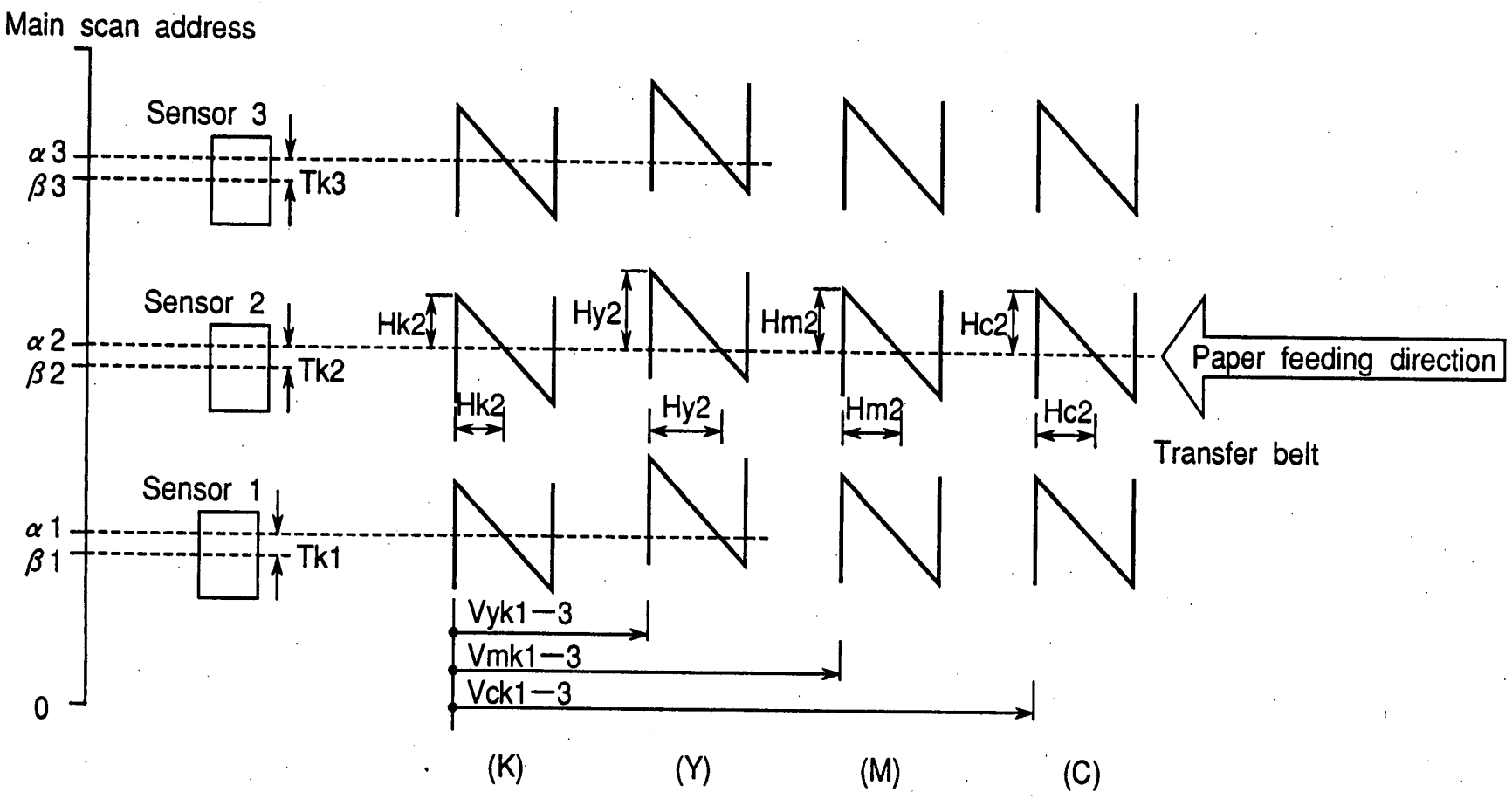

Main scan address
Sensor 3
α3
β3
Tk3
Sensor 2
α2
β2
Tk2
Sensor 1
α1
β1
Tk1
0
Hk2
Hy2
Hm2
Hc2
Hk2
Hy2
Hm2
Hc2
Paper feeding direction
Transfer belt
Vyk1−3
Vmk1−3
Vck1−3
(K)
(Y)
(M)
(C)

Fig.21

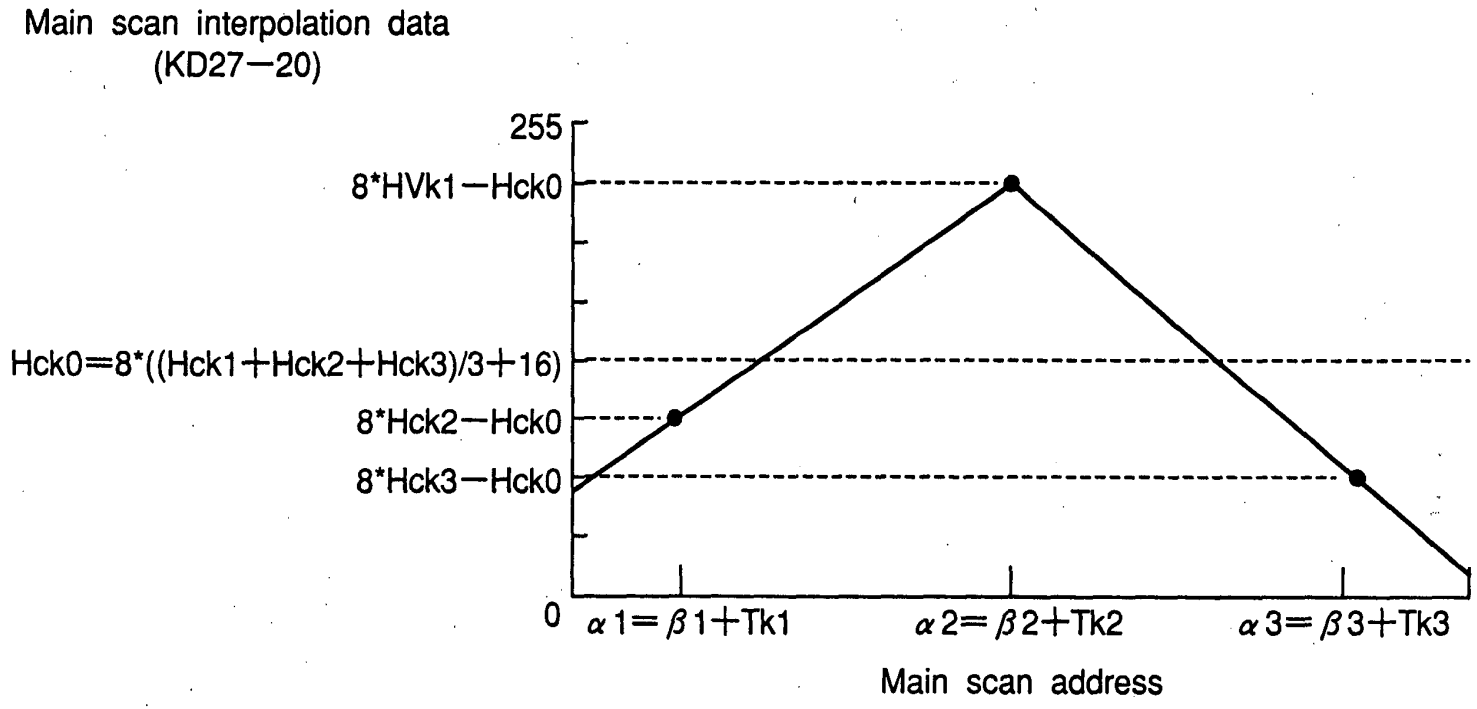

Main scan interpolation data
(KD27−20)
255
8*HVk1−Hck0
Hck0=8*((Hck1+Hck2+Hck3)/3+16)
8*Hck2−Hck0
8*Hck3−Hck0
0
α1=β1+Tk1
α2=β2+Tk2
α3=β3+Tk3
Main scan address

Fig.22

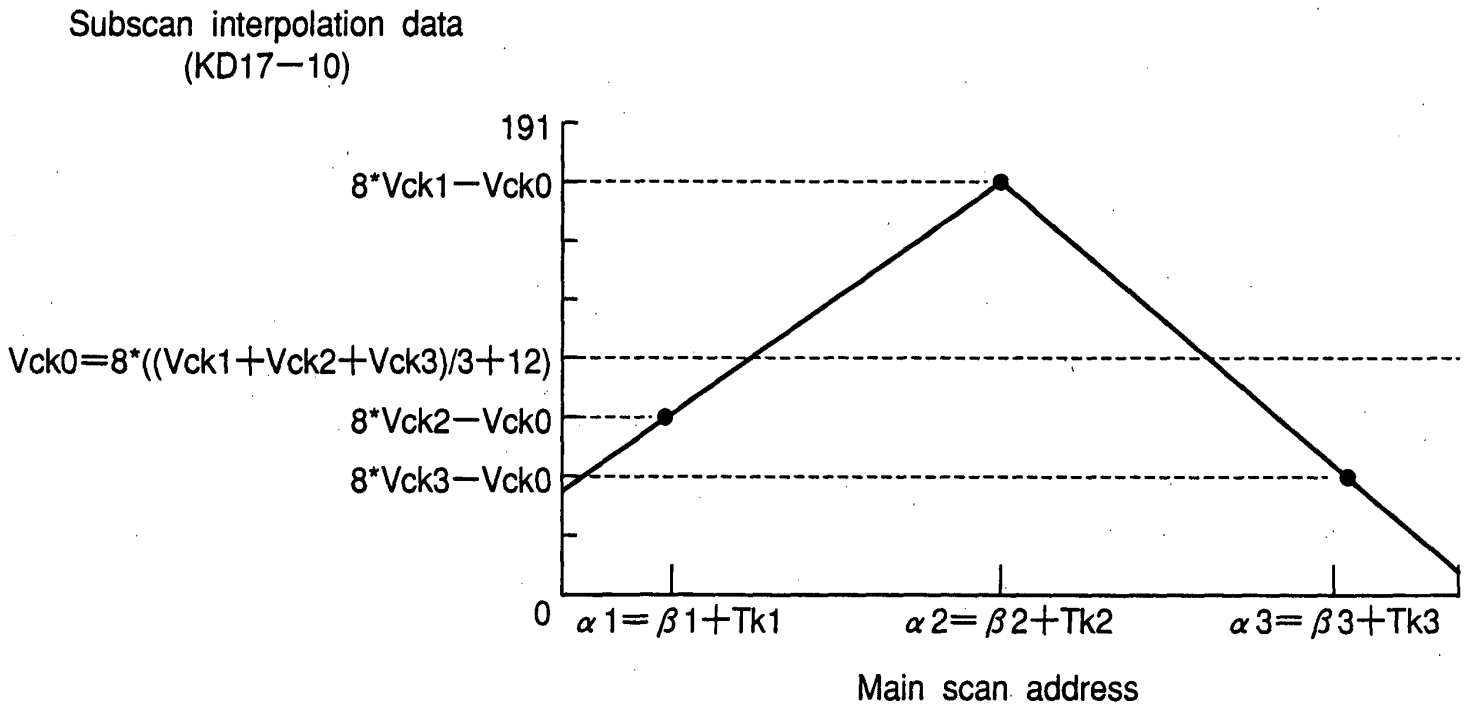

Subscan interpolation data
(KD17−10)
191
8*Vck1−Vck0
Vck0=8*((Vck1+Vck2+Vck3)/3+12)
8*Vck2−Vck0
8*Vck3−Vck0
0
α1=β1+Tk1
α2=β2+Tk2
α3=β3+Tk3
Main scan address

Fig.23

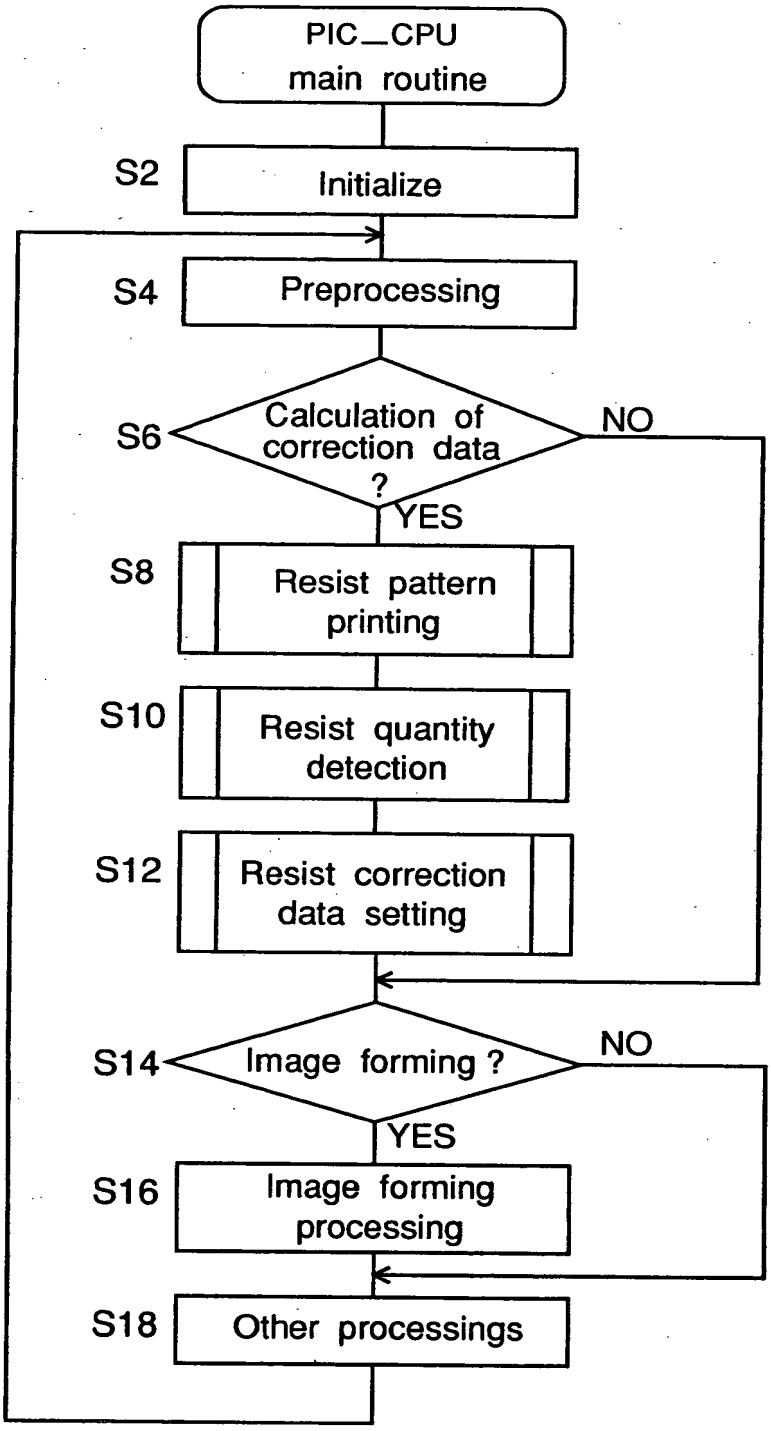

PIC_CPU
main routine
S2
Initialize
S4
Preprocessing
S6
Calculation of correction data ?
NO
YES
S8
Resist pattern printing
S10
Resist quantity detection
S12
Resist correction data setting
S14
Image forming ?
NO
YES
S16
Image forming processing
S18
Other processings

Fig.24

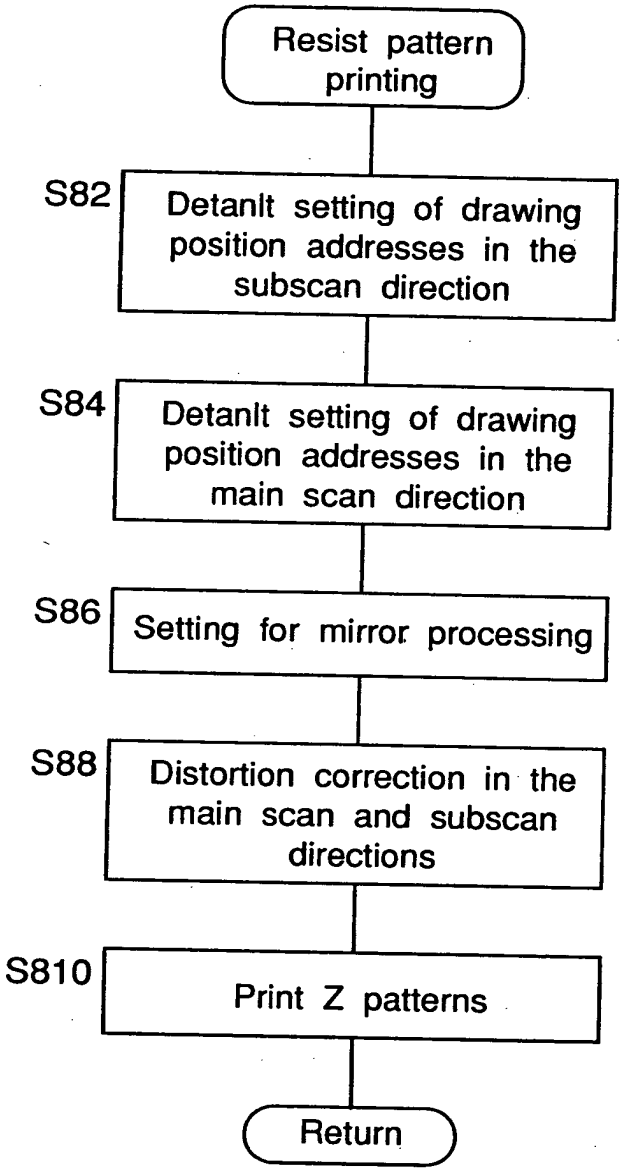

Resist pattern printing
S82
DetanIt setting of drawing position addresses in the subscan direction
S84
DetanIt setting of drawing position addresses in the main scan direction
S86
Setting for mirror processing
S88
Distortion correction in the main scan and subscan directions
S810
Print Z patterns
Return

Fig.25

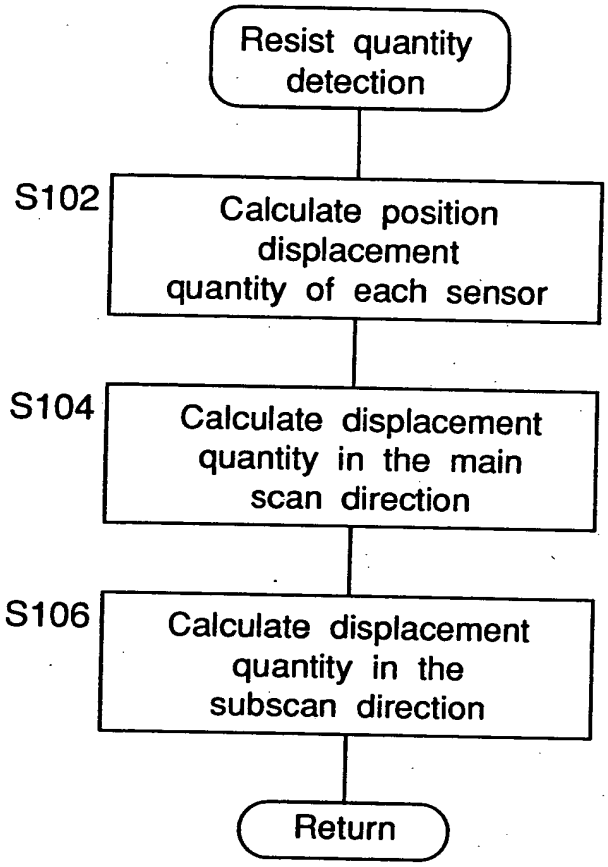

Resist quantity detection
S102
Calculate position displacement quantity of each sensor
S104
Calculate displacement quantity in the main scan direction
S106
Calculate displacement quantity in the subscan direction
Return

Fig.26

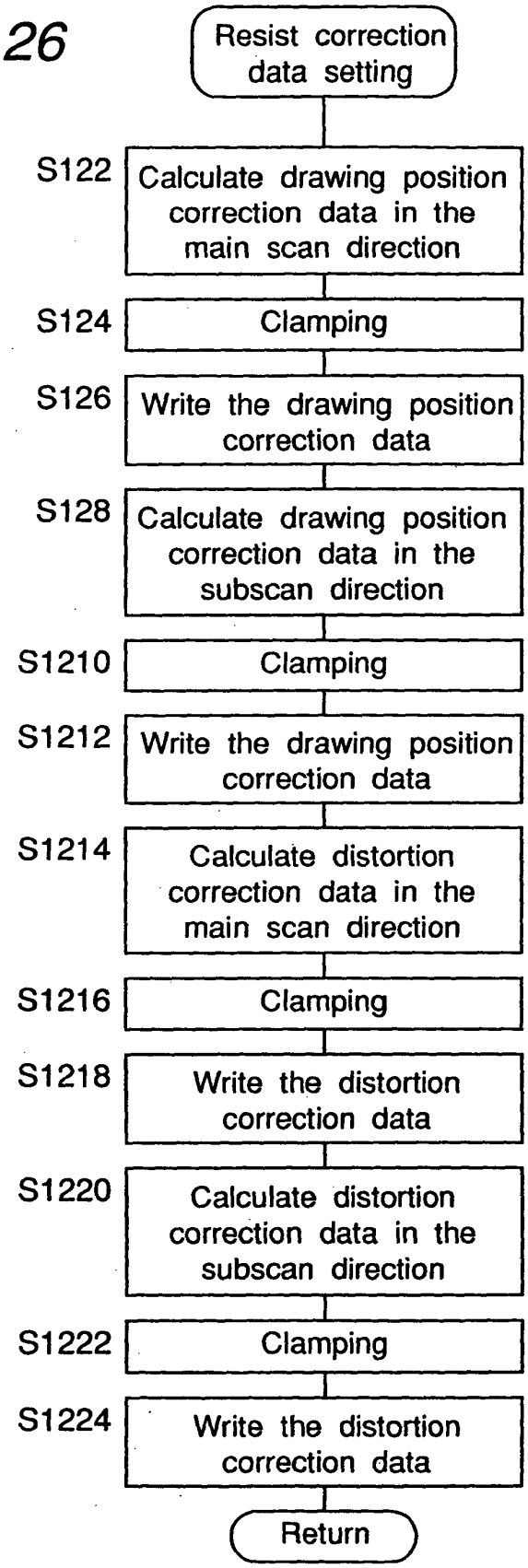

Resist correction data setting
S122
Calculate drawing position correction data in the main scan direction
S124
Clamping
S126
Write the drawing position correction data
S128
Calculate drawing position correction data in the subscan direction
S1210
Clamping
S1212
Write the drawing position correction data
S1214
Calculate distortion correction data in the main scan direction
S1216
Clamping
S1218
Write the distortion correction data
S1220
Calculate distortion correction data in the subscan direction
S1222
Clamping
S1224
Write the distortion correction data
Return

Fig.27A

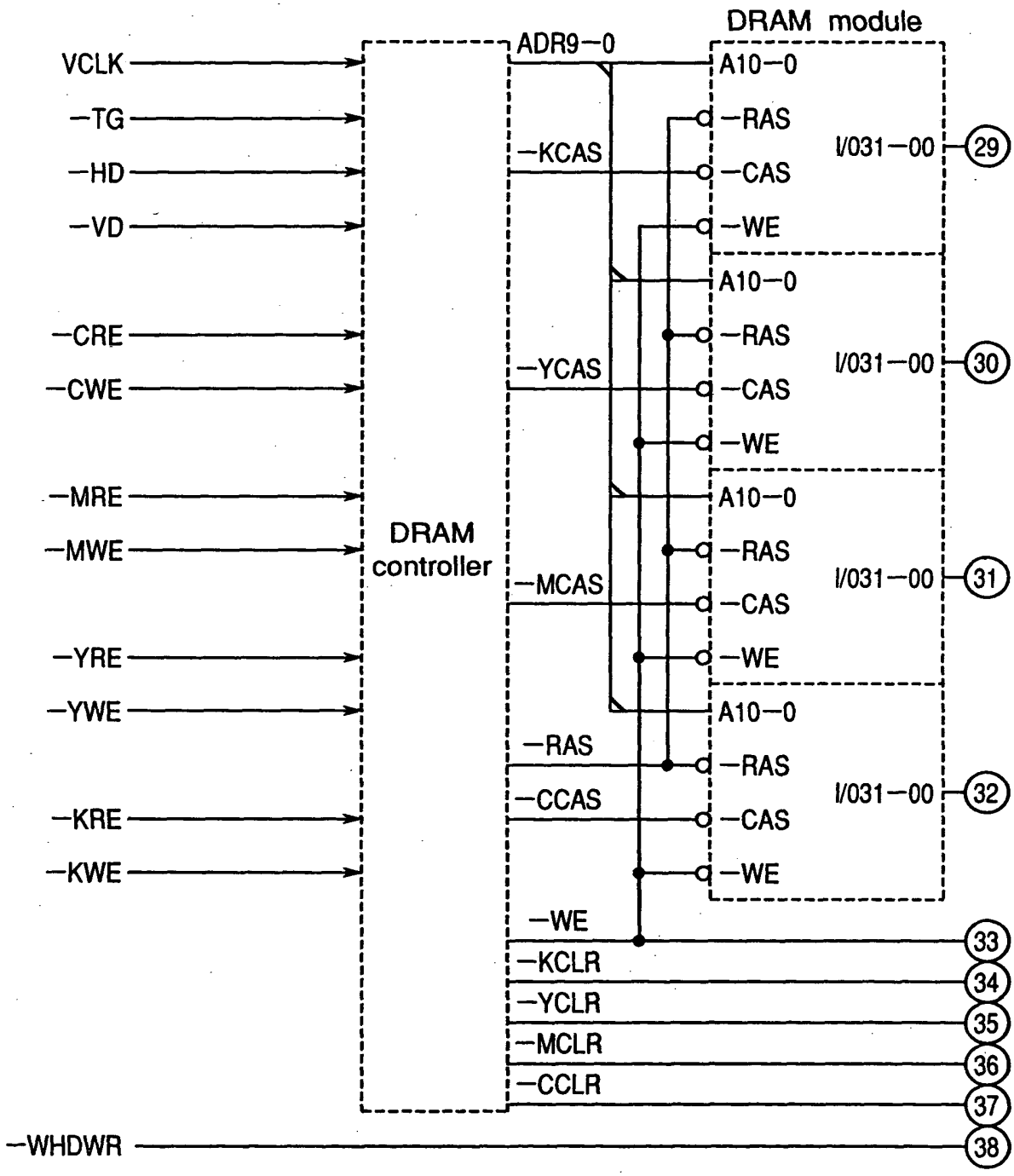
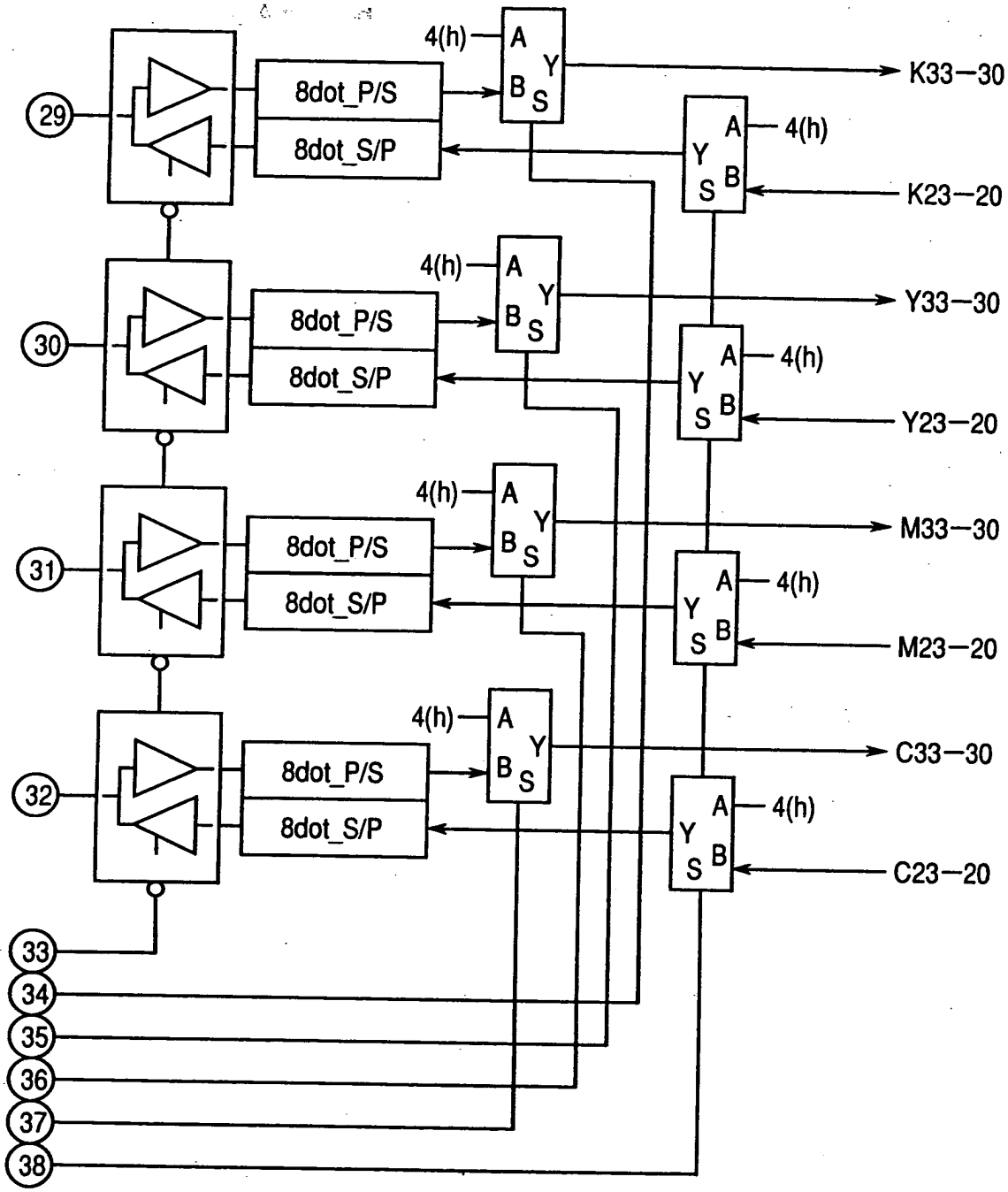

DRAM module
VCLK
−TG
−HD
−VD
−CRE
−CWE
−MRE
−MWE
−YRE
−YWE
−KRE
−KWE
DRAM controller
ADR9−0
−KCAS
−YCAS
−MCAS
−RAS
−CCAS
−WE
−KCLR
−YCLR
−MCLR
−CCLR
−WHDWR
A10−0
−RAS
−CAS
−WE
I/031−00
29
30
31
32
33
34
35
36
37
38

Fig.27B


29
30
31
32
33
34
35
36
37
38
8dot_P/S
8dot_S/P
4(h)
A
B
Y
S
K33–30
K23–20
Y33–30
Y23–20
M33–30
M23–20
C33–30
C23–20